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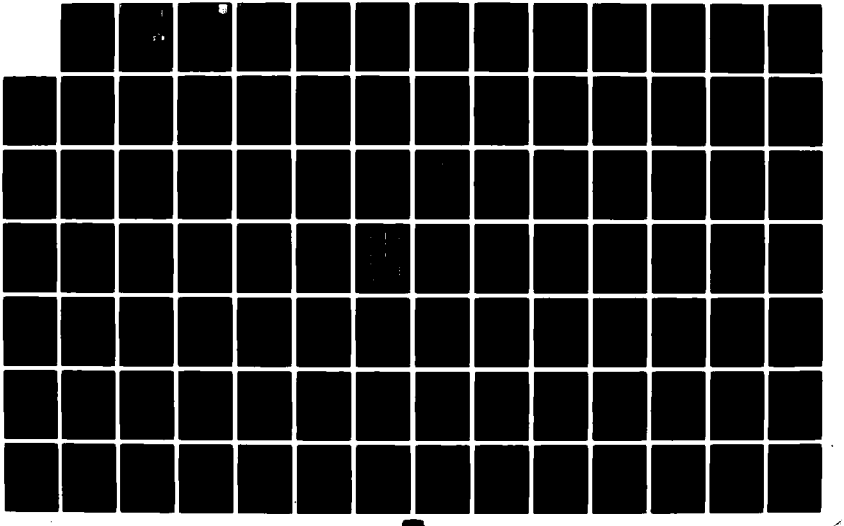

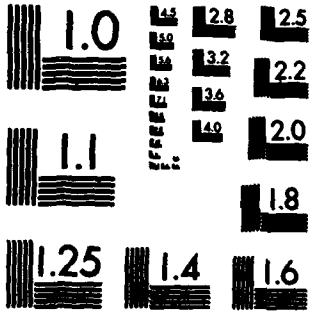

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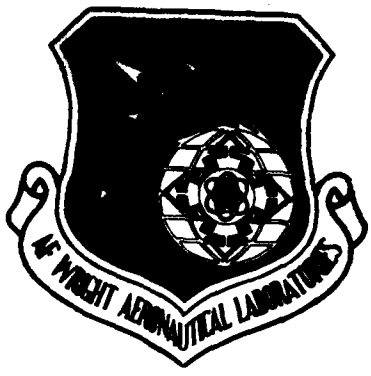

CRITICAL ITEM PRODUCT FUNCTION SPECIFICATION FOR THE MULTIPROCESSOR SHARED MEMORY (MSM)

JAHN A. LUKE, DAN WEISS, JERRY SHAW

JANUARY 1983

FINAL REPORT FOR THE PERIOD MAY 1979 - NOV 1982

AVIONICS LABORATORY
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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Multiprocessor Shared Memory, DECsystem-10, KI-10 processor, KL-10 processor, PDP-11 minicomputer, UNIBUS

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report is a specification that establishes the performance, design, and testing of the Multiprocessor Shared Memory (MSM). The MSM is a device that has been designed to supersede the DMA10, a direct memory access device built by the Digital Equipment Corporation (DEC). The MSM provides common memory for the DECsystem-10 (KI10 or KL10 processor) and the PDP-11 minicomputer (UNIBUS device). It also provides communications between processors and control. The MSM can configure up to four KI10 or KL10 processors and up to eight PDP-11's.

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1.0 SCOPE

This specification establishes the performance, design, test, manufacture and acceptance requirements for the Multiprocessor Shared Memory (MSM) critical item. The MSM is a device that has been designed to supersede the DMA10, a direct memory access device built by the Digital Equipment Corporation (DEC).

References to PDP-11 in this document mean the use of a UNIBUS-compatible device. DEC-10 is synonomous with DECsystem-10.

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. Unless otherwise indicated, the issue in effect on the date of invitation for bids or request for proposal shall apply.

2.1 Government Documents

Specifications: None

Standards:

MIL-STD-130	Identification and marking of U.S. Military property
MIL-STD-454E	Standard general requirements for electronic equipment
MIL-STD-490	Specification practices

Drawings:

DF*30698001	General Multiprocessor Shared Memory (MSM) Drawings
DF*30698002	Single Channel MSM (Prototype) Drawings
DF*30698003	Dual Channel MSM Drawings

Other Publications:

WF*30698002	Single Channel MSM (Prototype) Wire List Package

2.2 Non-Government Documents

The following Digital Equipment Corporation documents are relevant to this specification:

DECsystem-10 Hardware Reference Manual
DECsystem-10 Interface Manual
PDP-11 Peripherals Handbook
PDP-11 Processor Handbook
DMA10 Controller and Memory Link Interface

3.0 REQUIREMENTS

3.1 Item Definition

3.1.1 Multiprocessor Shared Memory (MSM)

3.1.1.1 Function

The MSM is a shared memory and interprocessor communications and control device. It can be configured to provide memory access ports for one to eight UNIBUS devices (i.e., PDP-11) and one to four DECsystem-10 processors. The MSM sequentially processes memory requests without regard to port priority and provides read data to any port within 200 nanoseconds of request recognition. The MSM has control and status registers for each UNIBUS device and DEC-10 processor. With these registers any DEC-10 Central Processing Unit (CPU) can configure any UNIBUS device and control its access to MSM memory. These registers also provide bidirectional interrupt communications between DEC-10 processors and UNIBUS devices.

3.1.1.2 Configurations

Each PDP-11 communicates with the MSM over its UNIBUS cable for both memory and register transfers. Each DECsystem-10 processor communicates with the MSM using one to four memory buses for memory transfers and one I/O bus for register transfers. The MSM can be configured for four-way interleaving by expanding the memory into four sections and connecting one to four DEC-10 CPU's, each in a four bus interleaved mode.* The MSM cannot be configured for any other interleaving scheme. The minimum MSM configuration interfaces to one UNIBUS, one DEC-10 memory bus, and one DEC-10 I/O bus. The maximum MSM configuration interfaces to eight UNIBUS's, sixteen DEC-10 memory busses, and four DEC-10 I/O busses.

3.1.1.3 Organization (Architecture)

The MSM consists of four subsystems: the Memory Subsystem (MS), the Interprocessor Communications Subsystem (ICS), the MSM Memory Bus, and the Status and Control Subsystem (SCS). The MS and ICS interface to the busses and contain the registers and memory.

The size of the MS and ICS depends on the number of DEC-10 processors and PDP-11's connected. The SCS, which monitors the status of the various subsystems, consists of a front panel and universal logic. The SCS size is the same regardless of the configuration. The MSM Memory Bus connects the ICS and MS together. Four MSM Memory Busses are required in interleaved mode. Figure 1 is the block diagram for the MSM.

* KL10 processor only

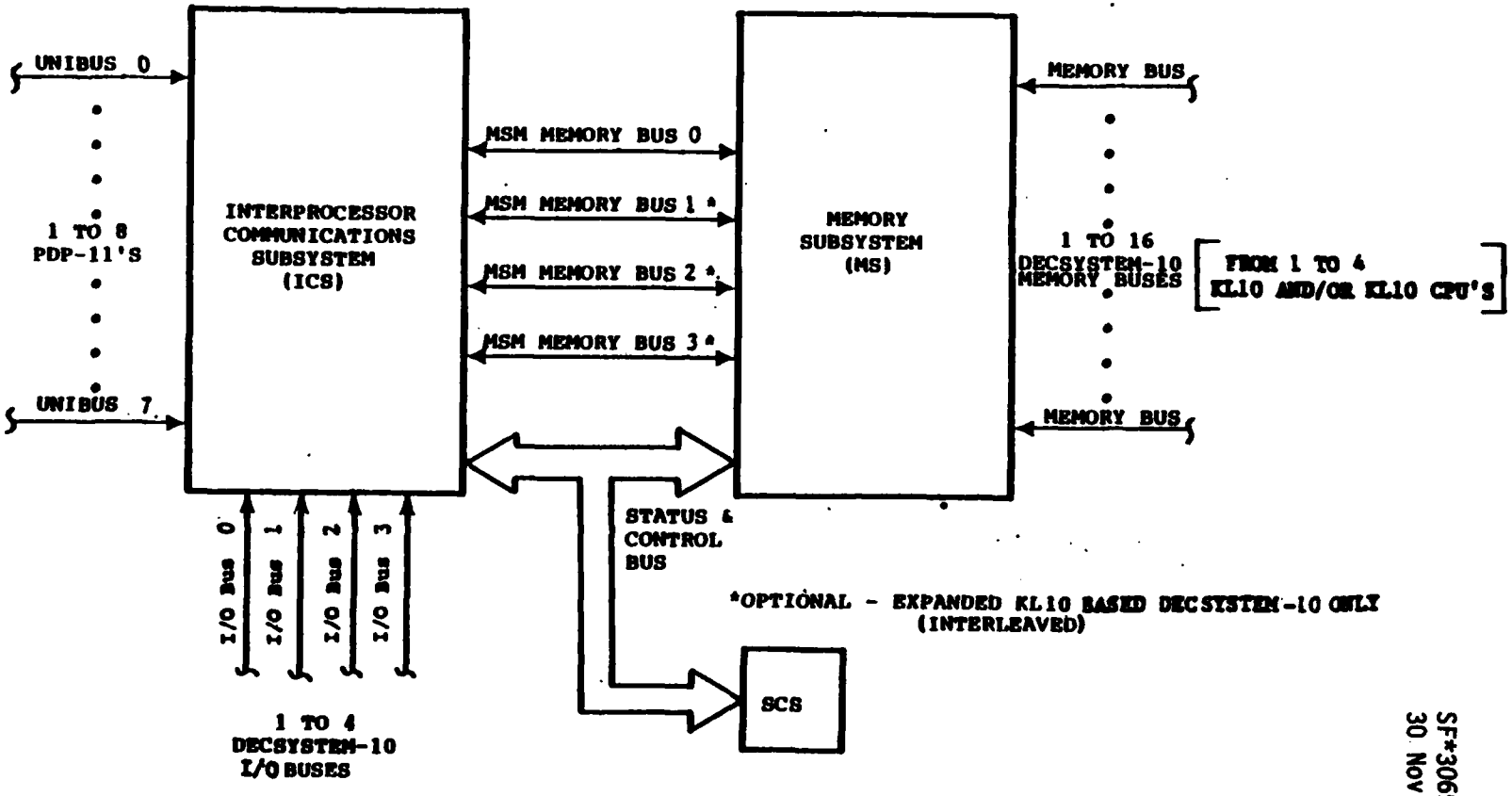

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Figure 1 Multiprocessor Shared Memory (MSM) Block Diagram

3.2 Characteristics

3.2.1 Performance

3.2.1.1 Memory Subsystem (MS)

The MS is made up of either one or four Memory Sequencer and Interface (MSI) modules. In noninterleaved mode, the MS consists of one MSI module. The MS can service one to four DEC-10 memory busses and one MSM Memory Bus in this mode. In interleaved mode, the MS consists of four MSI modules and services four MSM Memory Buses and four, eight, twelve, or sixteen DEC-10 memory busses depending on how many DEC-10 CPU's are connected. The Memory Subsystem is not defined for two or three MSI configurations.

3.2.1.1.1 Memory, Sequencer, and Interface (MSI)

The MSI consists of the Solid State Memory (SSM), Memory Access Sequencer (MAS), and one to four Memory Bus Interface (MBI) modules (Figure 2).

3.2.1.1.1.1 Solid State Memory (SSM)

The SSM (Figure 3) is the heart of the MSM system. It is arranged in 16K blocks of 40-bit words (thirty-six data bits and four parity bits). Each SSM can be expanded in 16K steps to 128K words of memory. A four-MSI interleaved configuration can contain 128K per MSI module or a maximum of 512K 40-bit words. Seventeen address bits, A0 to A16, are required to address the 128K of SSM in each MSI module.

The SSM uses a 35 nanosecond access time, 4K x 1 static HMOS RAMS with deselect powerdown. Each 16K block of SSM is implemented on a single circuit board and is interchangeable with any other SSM board in the system. This interchangeability is implemented by decoding A14 to A16 in the MAS and bringing out eight slot select lines to enable the slots. Also, each board is divided internally into 4K x 40 banks. Address bits A12 and A13 are decoded in the MAS and four bank select lines are sent to each slot. A0 to A11 connect directly to each 4K RAM segment. During any memory access, only a 4K x 40 (40 IC's) slice of memory will be in the active (powered-up) mode. The rest of memory will be in the power saving standby mode. The SSM also has an "I AM HERE" output signal that allows the number of 16K blocks to be determined.

The DEC-10 processor uses a 36-bit data word. When it transfers data on the memory bus it adds one parity bit for a total of 37 bits. The PDP-11 processor uses a 16-bit data word and no parity bits. The PDP-11 can write 8-bit bytes or 16-bit words to memory. To accomodate DEC-10 data and word length the SSM is 36 data bits wide. Since the PDP-11 can write 8-bit bytes, the SSM has four parity bits, one for each byte. Thirty-six data bits do not divide evenly into four bytes so the partitioning in Figure 3 is utilized. A DEC-10 word (D0 to D35) is separated into two groups of

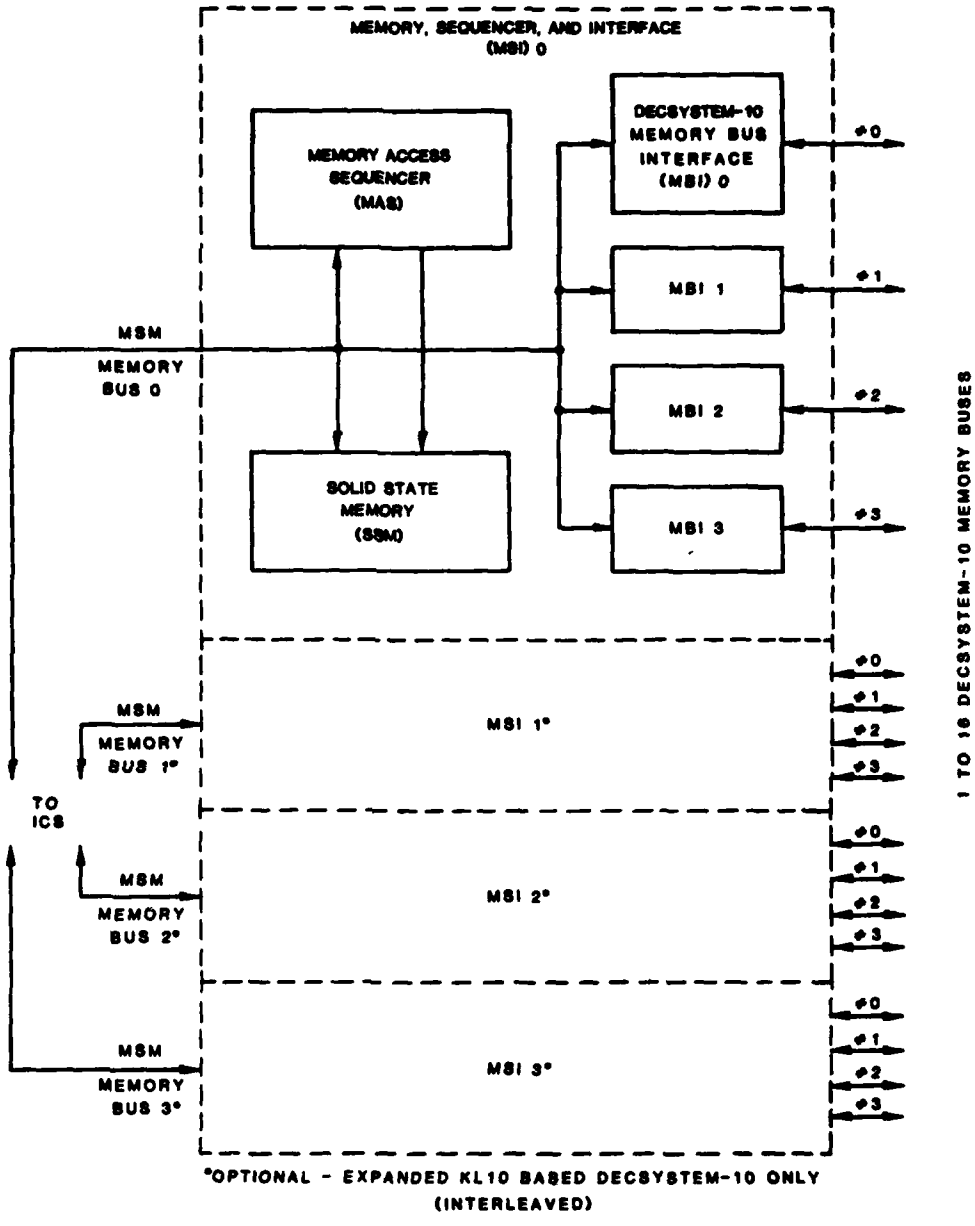


Figure 2 Memory Subsystem (MS) Block Diagram

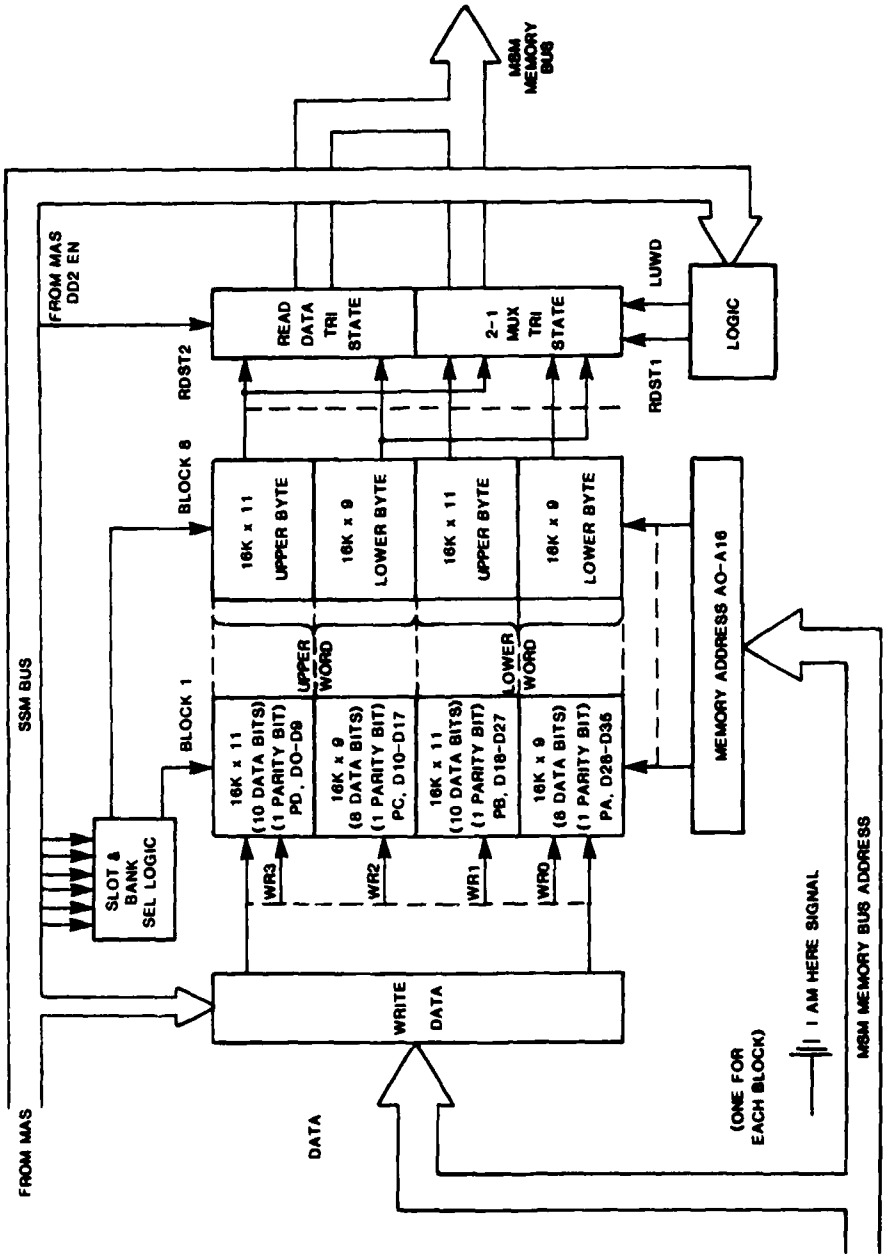


Figure 3 Solid State Memory (SSM) Block Diagram

ten and two groups of eight bits (D0 to D9, D10-D17, D18-D27, and D28 to D35). Parity bits are generated in the source ports and stored for each group. A PDP-11 byte or word (two bytes) must be extended to fill up the 10-bit data groups. This is accomplished by putting zeros or extending the sign (MSB) into the two unused positions. The technique depends on how a controlling DEC-10 CPU has configured the accessing PDP-11 channel. Each data group is individually accessible using control lines from the Memory Access Controller (MAC). Figures 3a-3e depict the word partitioning and parity generation scheme for the MSM.

3.2.1.1.1.2 Memory Access Sequencer (MAS)

The MAS is a sequential scanner which scans request lines from the various ports and grants SSM access to one port at a time. Each MSI module serves up to four DEC-10 memory busses and eight PDP-11 channels. The MAS scans all twelve ports in a circular fashion without regard to port priority (Figure 4). The MAS always scans twelve ports whether or not hooked up or active. The MAS scans at a 20MH$_z$ rate and requires 50ns to check each request line and 600ns to complete a scan. When a request is recognized the multiple access sequencer locks on the appropriate port. It will release the port and resume scanning within 200ns, if the request is for a read or write operation. For a read-modify-write operation, the time depends on the speed of the DEC-10 instruction.

The MAS latches and decodes port control lines, interfaces the MSM Memory Bus to the SSM, and generates timing and control signals to sequence the SSM. No port control lines go directly to the SSM. A DEC-10 port operation always transfers thirty-six data bits and four parity bits, so one DEC-10 word translates directly to one MSM memory word. However, a PDP-11 port operation can include byte and word transfers. Therefore, PDP-11 data can be transferred to and from the different data subgroups within an MSM memory word. The PDP-11 can be configured to store data in 1-1 or 2-1 memory mode (one or two PDP-11 words in each MSM memory word). The control signals emanating from the different ports to the MAS are listed in Table I. The control signals emanating from the MAS to the SSM are listed in Table II. There are fifteen different SSM access modes (Table III) that require the MAS to generate unique control functions.

The MAS latches address and data bits and provides the slot and bank select lines to the SSM. If a DEC-10 read-modify-write instruction is not terminated within 25μs, the MAS sends an error signal to the DEC-10 port and continues scanning. The "I AM HERE" lines from each 16K memory card are encoded in the MAS and transmitted to the SCS to calculate the total number of 16K memory blocks in the MSM. The MAS has a flip-flop for each grant line to "remember" which port last received service. It has tri-state drivers to transmit this and other information to the SCS. The MAS on one board is interchangeable with any other MAS board.

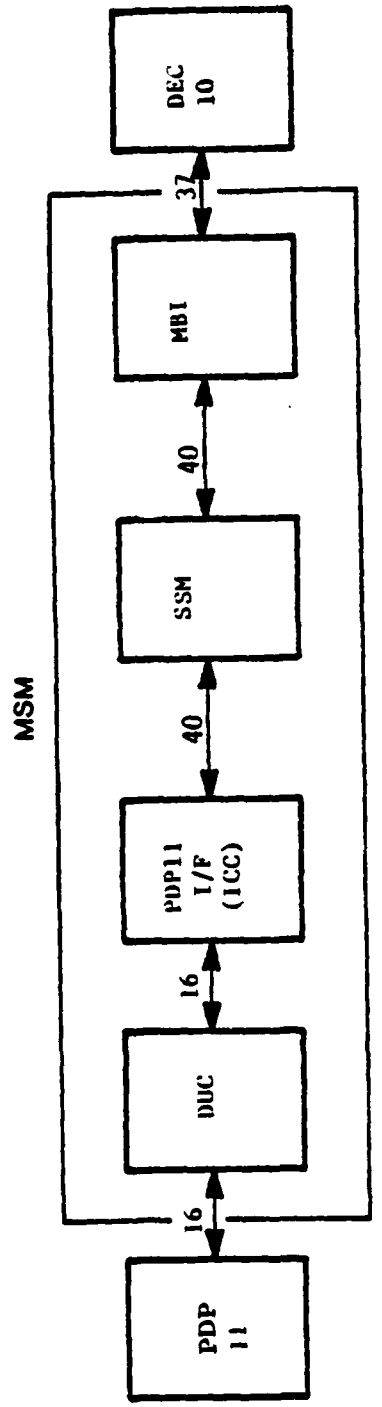


Figure 3a MSM Parity Scheme

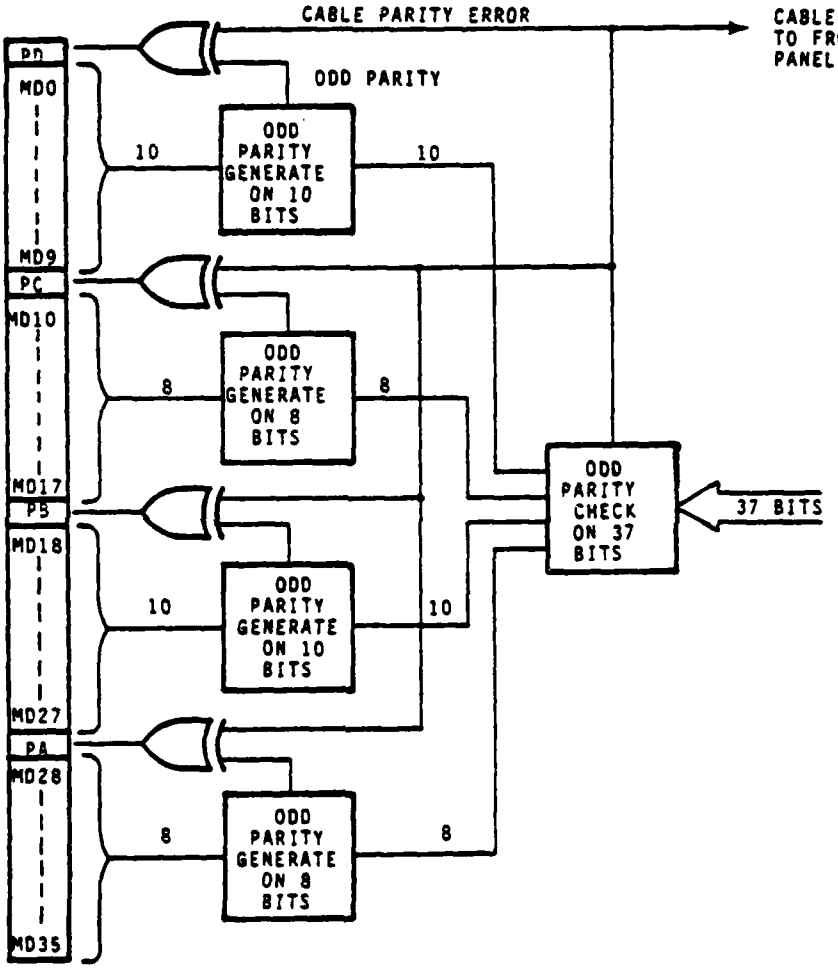


Figure 3b DEC-10 Writes to MSM

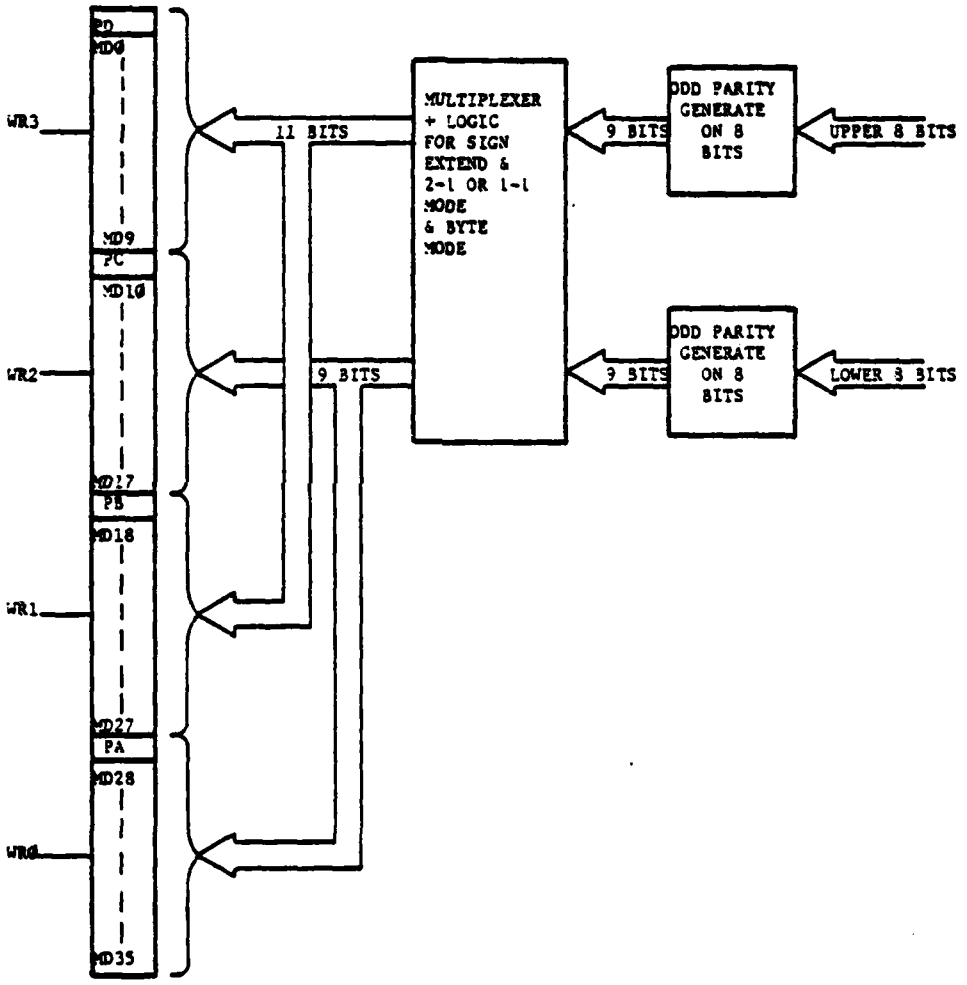


Figure 3c PDP-11 Writes to MSM Memory

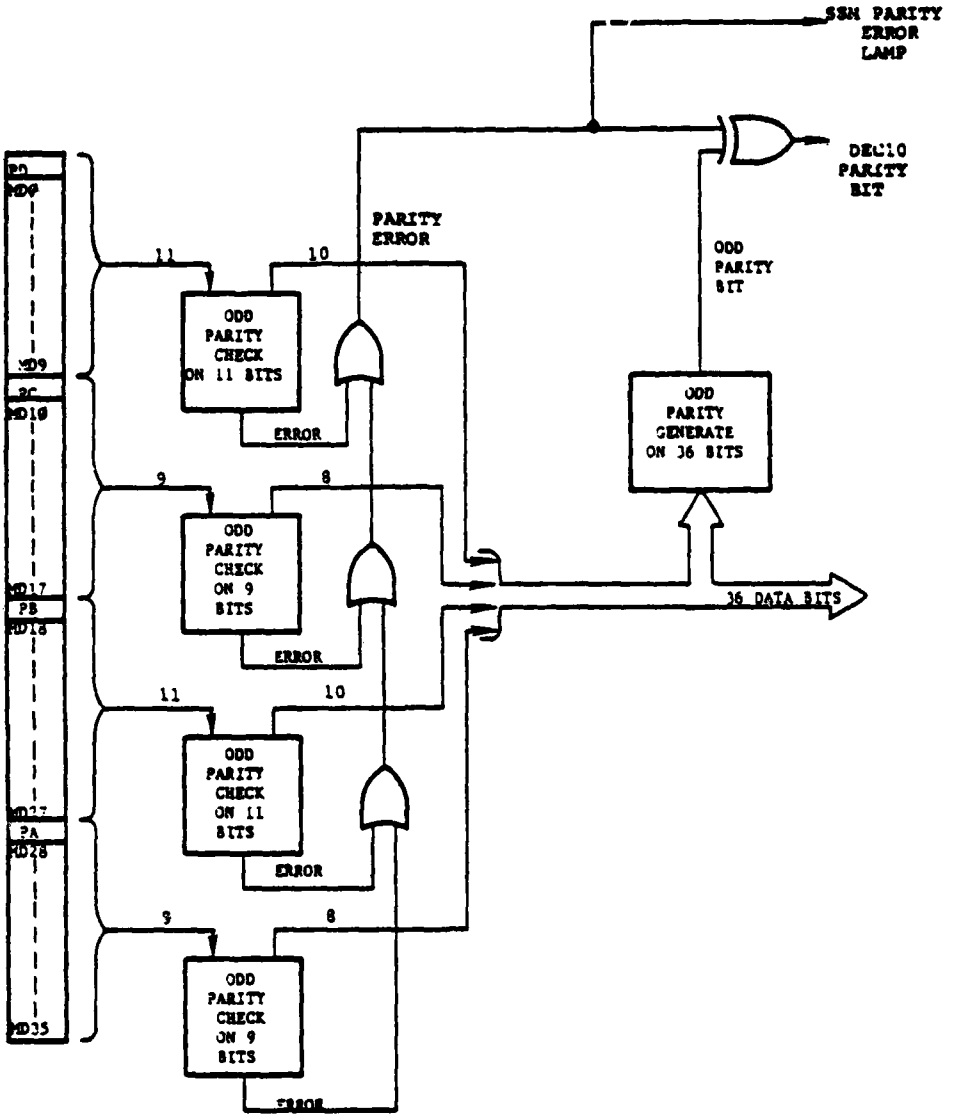


Figure 3d DEC-10 Reads MSM Memory

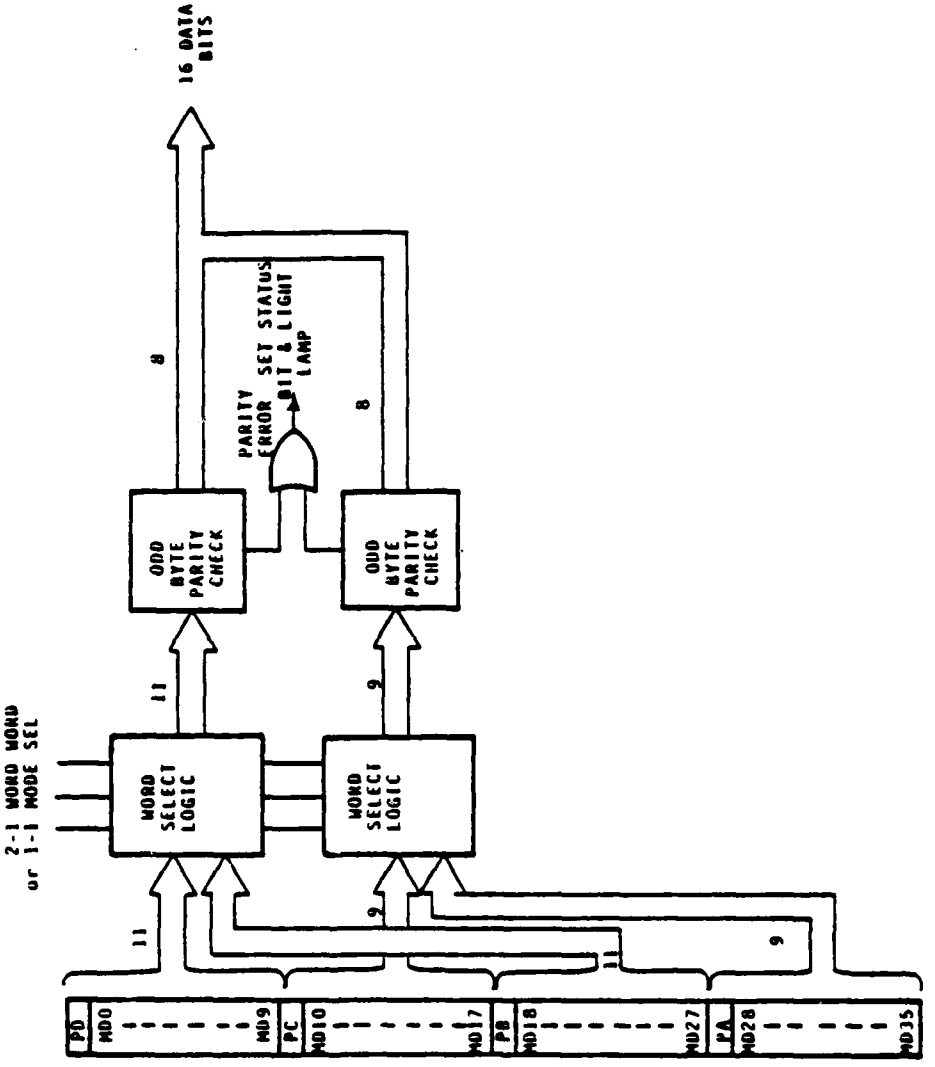


Figure 3e PDP-11 Reads MSM Memory

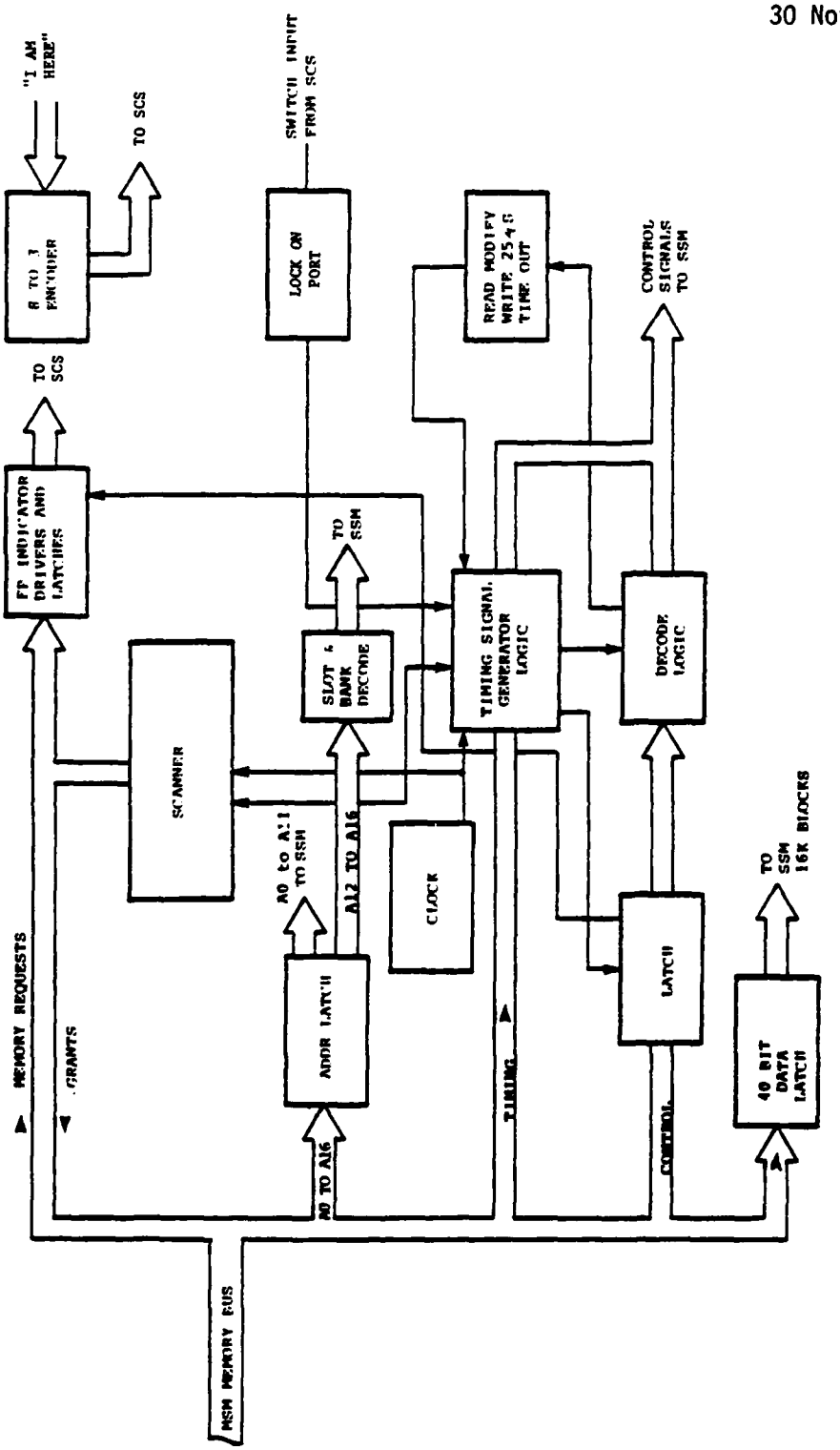


Figure 4 Memory Access Sequencer (MAS) Block Diagram

3.2.1.1.1.3 DEC-10 Memory Bus Interface (MBI)

The MBI (Figure 5) interfaces the DEC-10 memory bus to the MSM Memory Bus. The MBI electrically translates the DEC-10 memory bus levels to TTL levels, latches the 22-bit address (A14-A35) and control lines, provides the address range comparison, and accomplishes the MSM parity checking/generation. The 16K boundary start address, which comes from eight switches on the front panel, is subtracted from the DEC-10 address bits. The DEC-10 address must be greater than the 16K start address or the MBI will not respond to the memory bus request. When the MSM is in interleaved mode, the two low order address bits (A34 & A35) are ignored since each DEC-10 memory bus is interleaved according to A34 & A35.

The MBI manipulates the DEC-10 address to obtain a 17-bit address which is compatible with the SSM. Initially, the DEC-10 16K start address is subtracted from the DEC-10 address bits A14-A21. The new net address is run into a 2-1 multiplexer. If the MSM is in interleaved mode, address bits A34 & A35 are shifted out and address bits A17 to A33 to become the net address. In noninterleaved mode, no shift occurs and address bits A19-A35 are the net address. If this address is less than or equal to the upper 16K limit, this address is valid. Essentially, two conditions must be met for the MBI to respond to the DEC-10 memory bus:

1. The address must be greater than the 16K starting boundary.

2. The resulting address, after the 16K boundary is subtracted and interleave shifting occurs, must be less than the upper 16K limit derived in the SCS.

Throughout the DEC-10 and MSM memory, odd parity is used to define good data. During a write operation, the DEC-10 transmits 36 data bits and one odd parity bit to the MSM. The MBI checks these 37 bits for odd parity. To make this data compatible with the SSM format, the data is broken into groups as previously discussed. If the MBI detects a parity error in the data from the DEC-10, even parity, i.e. bad data, will be generated for each group.

During a DEC-10 read operation 40 bits (data and parity) are transferred from the SSM to the MBI. Each group of eleven and nine bits is checked for odd parity. To make the data compatible with the DEC-10, the MBI generates an odd parity bit for the 36 data bits. If any of the data groups read from the SSM were found to have even parity, the 37th bit (parity) will be made even, i.e. bad data. The data and parity bits are transmitted back to the DEC-10 where a parity error will be detected.

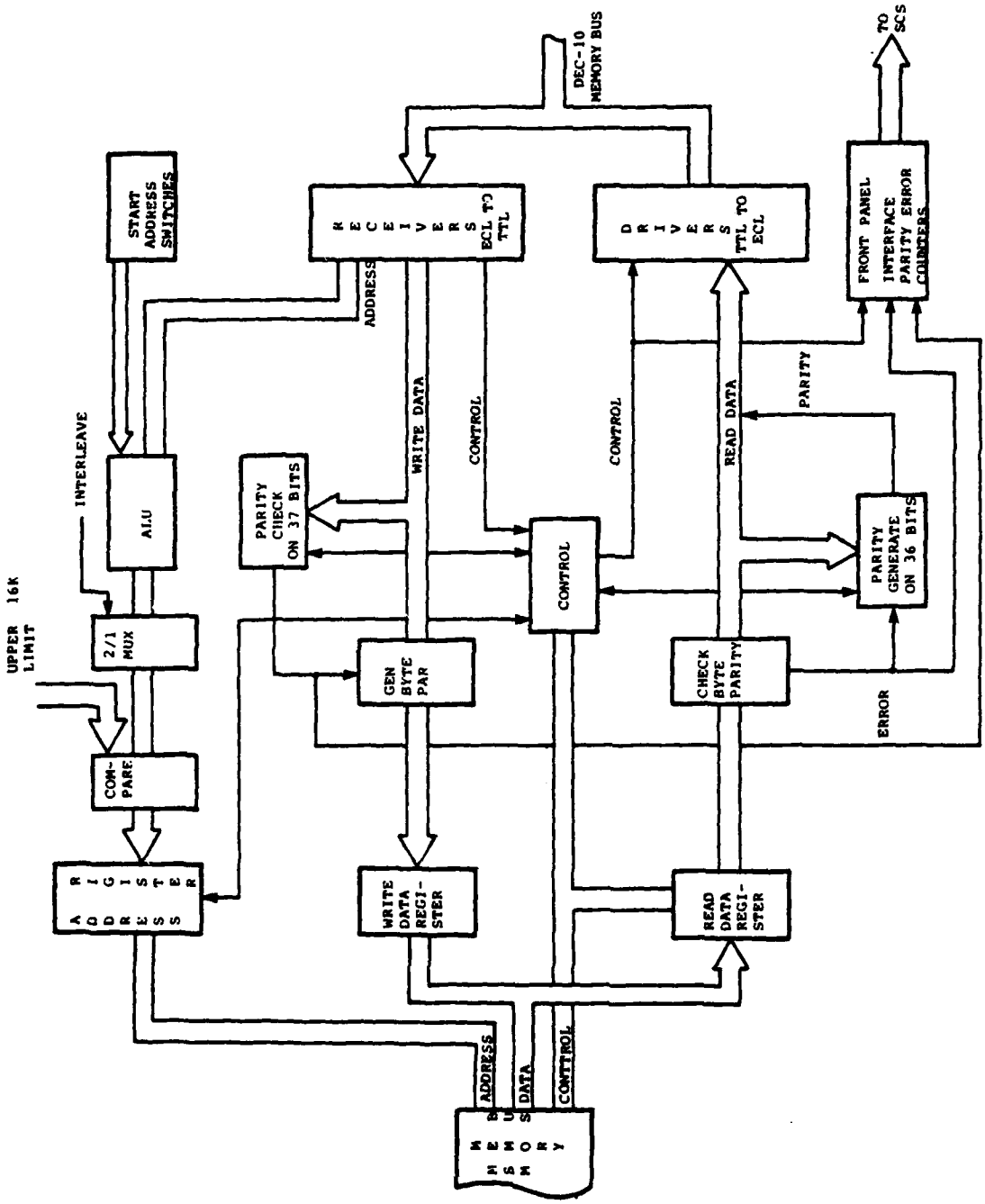


Figure 5 DEC-10 Memory Bus Interface (MBI) Block Diagram

The DEC-10 processor has three operating modes (fast, slow, and immediate) depending on the type of memory attached to its memory bus. For fast and slow memories the memory bus overlaps memory fetch cycles; while one memory location is returning data, another location can be addressed. For immediate memories fetch cycles are never overlapped. The DEC-10 has three different memory request lines and two address acknowledge lines. The MSM is wired to either the "fast request" or "immediate request" line and to the "address acknowledge untimed" line. The MSM is regarded as an immediate memory to the DECsystem-10.

The MBI has read and write parity error counters, stop on error logic, error detection logic, and status indicator drivers. These circuits are controlled and monitored by switches and displays on the front panel.

Each MBI consists of one circuit board which is interchangeable with any other MBI board. To add a DEC-10 memory bus to the MSM only requires installing another MBI card to a prewired slot in an MSI.

3.2.1.2 MSM Memory Bus

The MSM Memory Bus is used solely to transfer data between the SSM and the memory ports. The MSM Memory Bus signals showing source and destination are listed in Table IV. There are 91 lines of which 40 are data and parity, 17 are address, 24 are request-grant lines, and ten are control lines.

One or four MSM Memory Busses connects the ICS, to the MS. In the ICS the bus connects to each PDP-11 port (channel) and, in the MS, it connects one MSI module. In an MSI module it connects the MAS, SSM, and one to four MBI's (DEC-10 ports). If the MS is interleaved and consists of four MSI modules, one MSM Memory Bus connects each MSI to each PDP-11 port in the ICS. Each PDP-11 port is capable of accessing any MSI, but each DEC-10 port can only access the MSI module to which it is connected. Figure 6 shows the MSM Memory Bus cabling for a fully expanded MSM system.

3.2.1.2.1 DEC-10 Memory Bus Cabling

There are three kinds of DEC-10 CPU's: the KA10, KI10, and KL10. The MSM operates with the KI10 and KL10. The KI10 operates only in one bus mode, while the KL10 operates in one, two, or four bus modes. In multibus mode, the KL10 sends out address, data, and control signals on each bus simultaneously and divides the address according to the number of busses. Addresses ending in zero are always on bus zero, addresses ending in one are always on bus one, etc. If a memory can simultaneously respond to each bus, memory throughput is enhanced. For the MSM to enhance memory throughput, each of the DEC-10 memory busses from the same DEC-10 CPU in the four bus mode must be connected to a different MSI module. The MAS, in each MSI, independently responds to port requests. A one MSI module system will handle one DEC-10 CPU in a four bus mode, but each bus will be serviced sequentially rather than simultaneously and no time savings will result.

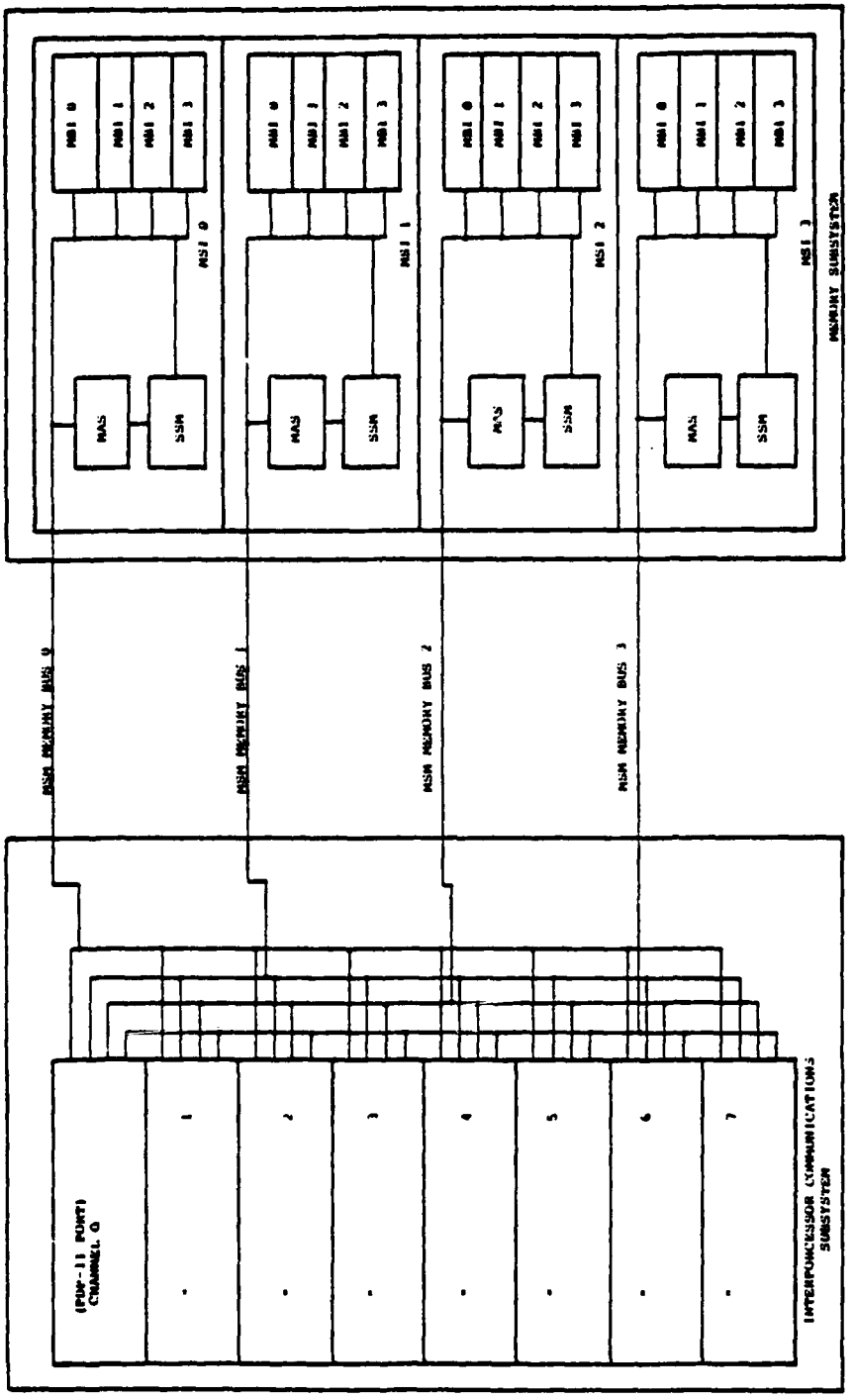


Figure 6 MSM Memory Bus Interconnects

When the MSM has four MSI modules, its memory is four-way interleaved. The memory in MSI 0 is only accessed if the address received at the memory port ends in zero. It follows that MSI's 1, 2, and 3 are only accessed if the addresses received at their memory ports end in one, two, and three, respectively (Figure 6). Each PDP-11 port determines which MSM Memory Bus to access by examining the three least significant bits of the address. The four DEC-10 memory ports can only access the MSI modules to which they are connected. Therefore, when in four bus mode, the DEC-10 memory bus must be cabled to the MSI number corresponding to its bus number. The MSM can support many DEC-10 memory bus cabling arrangements. A one MSI system supports: one to four KI10's and/or one to four KL10's in one bus mode, two KL10's in two bus mode, one KL10 in two bus mode and one or two KI10's or KL10's in one bus mode and one KL10 in four bus mode. A four MSI system supports one to four KL10's, each in four bus mode. Figures 7 through 11 illustrate the possible DEC-10 memory bus cabling arrangements.

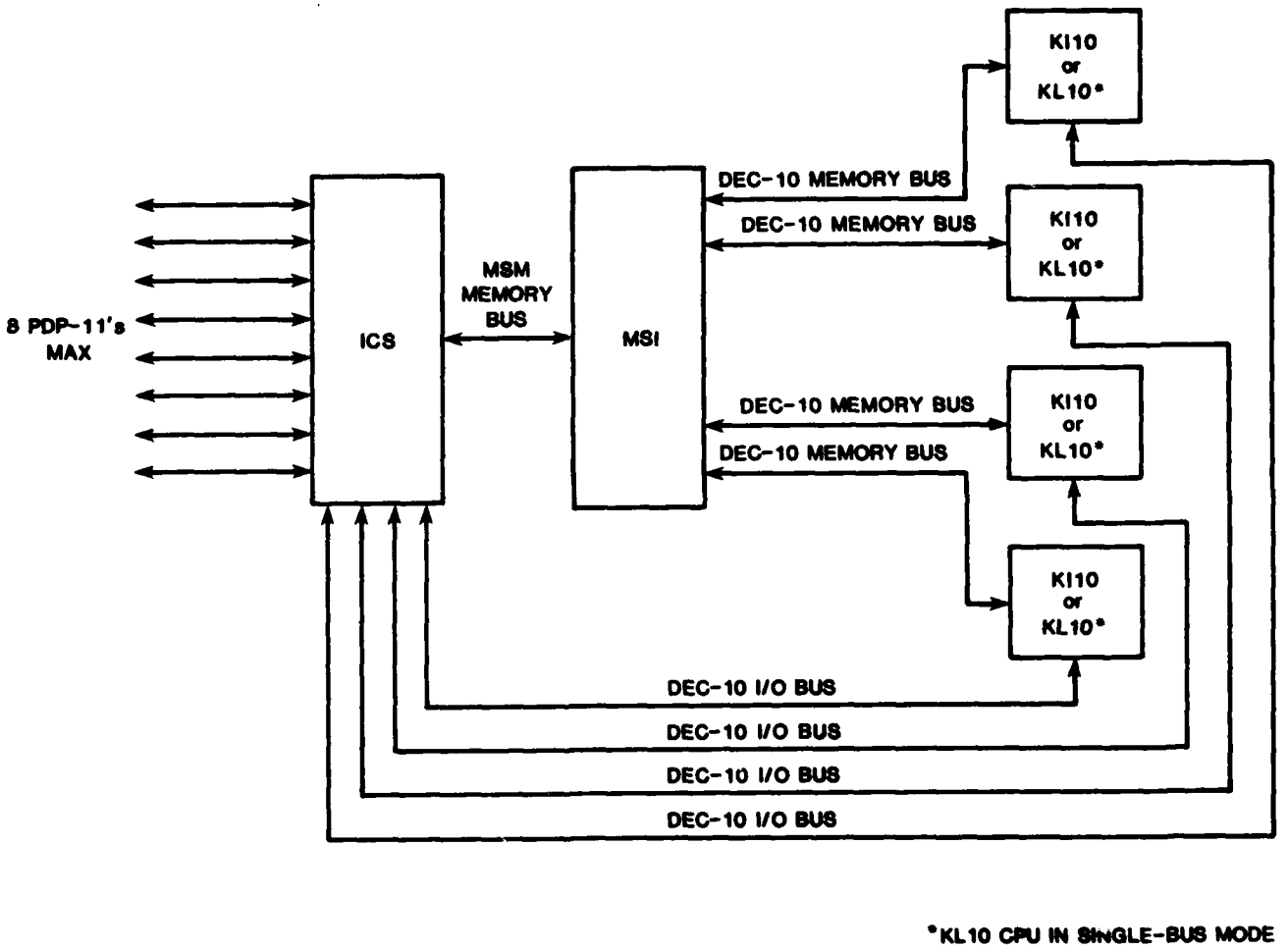
3.2.1.3 Interprocessor Communications Subsystem (ICS)

The ICS consists of from one to eight channels, one to four I/O Bus Interfaces (IOBI), and one to four ICS I/O Busses. The channels connect a PDP-11 UNIBUS to the MSM and act as a PDP-11 memory port to the MAS. There is one channel for each PDP-11. An IOBI connects a DEC-10 I/O bus to the MSM. The ICS I/O Bus connects each IOBI to every channel (Figure 12).

The channels allow PDP-11's controlled access to MSM memory. The access is controlled by a CPU which communicates with the channel over its DEC-10 I/O bus through an IOBI and ICS I/O Bus. The channels have memory mapping RAM's and registers. These alter the address and data transmitted between PDP-11's and MSM memory and permit channel access control by the DEC-10. These registers and RAM's are loaded via the DEC-10 I/O bus. There can be four DEC-10 processors in an MSM system, but each channel can be controlled by only one CPU at a time.

To keep several DEC-10 processors from attempting to access the same channel, a CPU must seize control of the channel. No other CPU can seize this channel until the seizing CPU releases it. One CPU can seize several channels provided the channels are not already seized by another CPU. If a seizing CPU is hung up or the program has failed, any other CPU can release all channels seized by the hung up CPU. This feature prevents channels from being hung up and is only used in emergencies.

The ICS also allows interprocessor communications and bidirectional interrupt capabilities. When a DEC-10 CPU generates an interrupt, it specifies which of its seized channels should be interrupted. When a PDP-11 generates an interrupt, it is sent to the DEC-10 CPU which has its channel seized. When a DEC-10 CPU writes registers, it specifies which of its seized channels contains the registers. A PDP-11 only accesses registers in the channel to which it is connected.



*KL10 CPU IN SINGLE-BUS MODE

Figure 7 Single MSI MSM Case 1

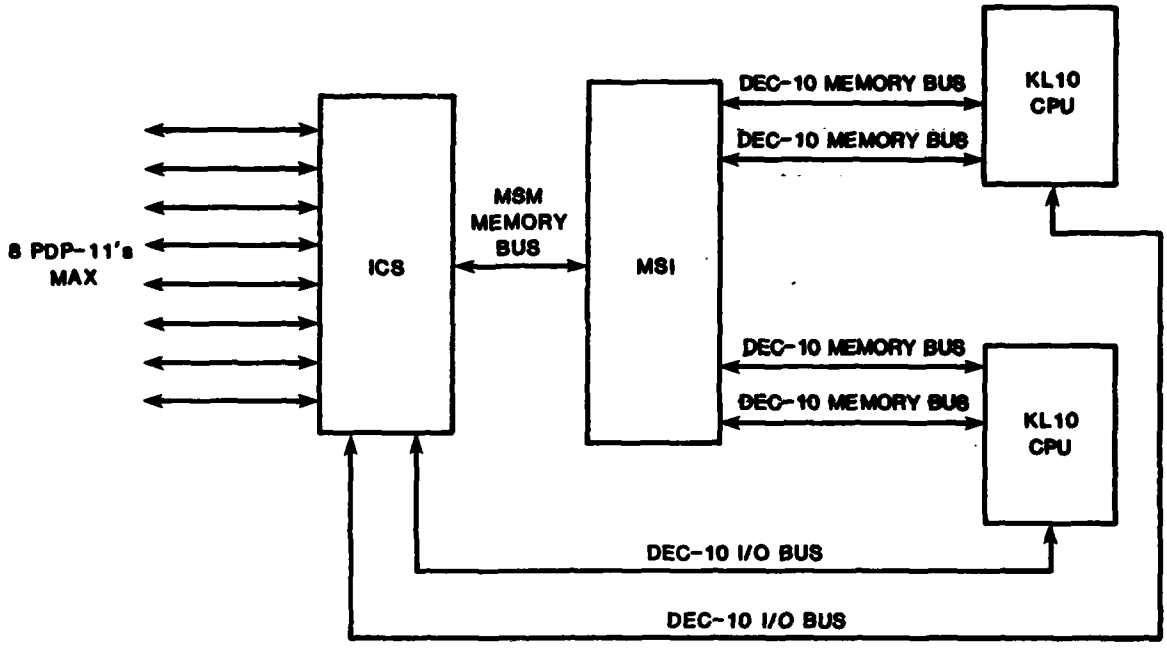
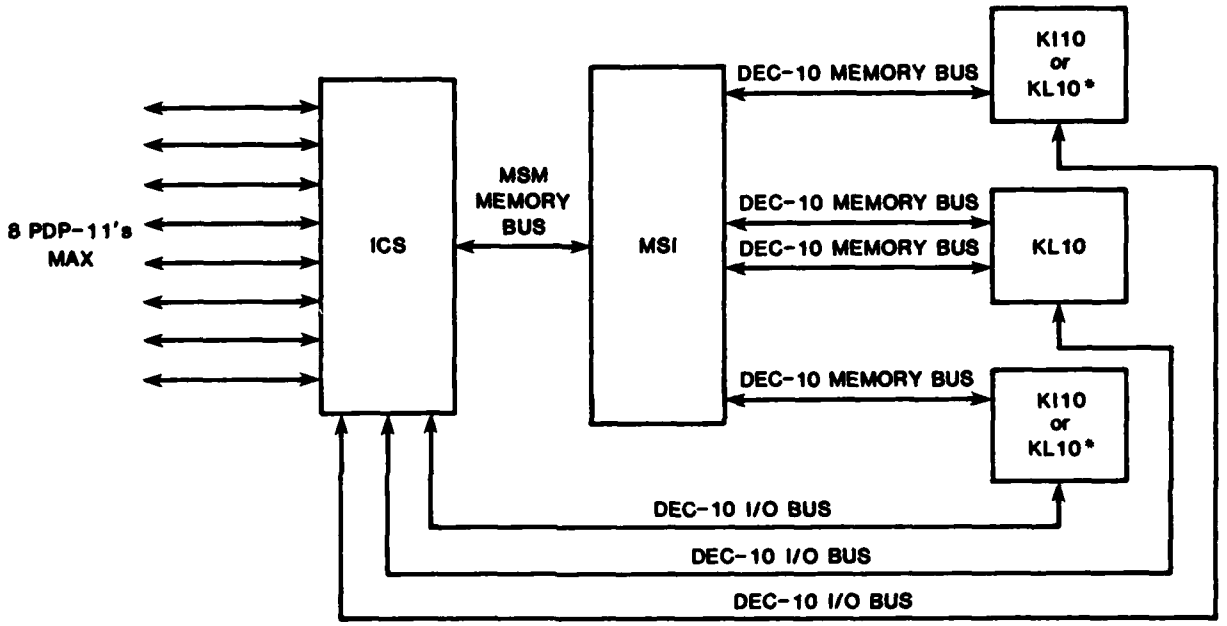


Figure 8 Single MSI MSM Case 2



*KL10 CPU IN SINGLE-BUS MODE

Figure 9 Single MSI MSM Case 3

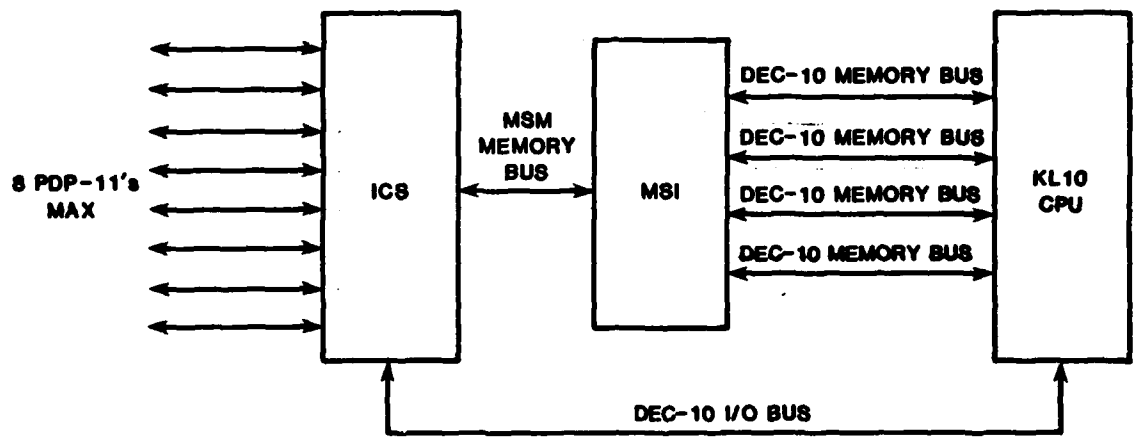


Figure 10 Single MSI MSM Case 4

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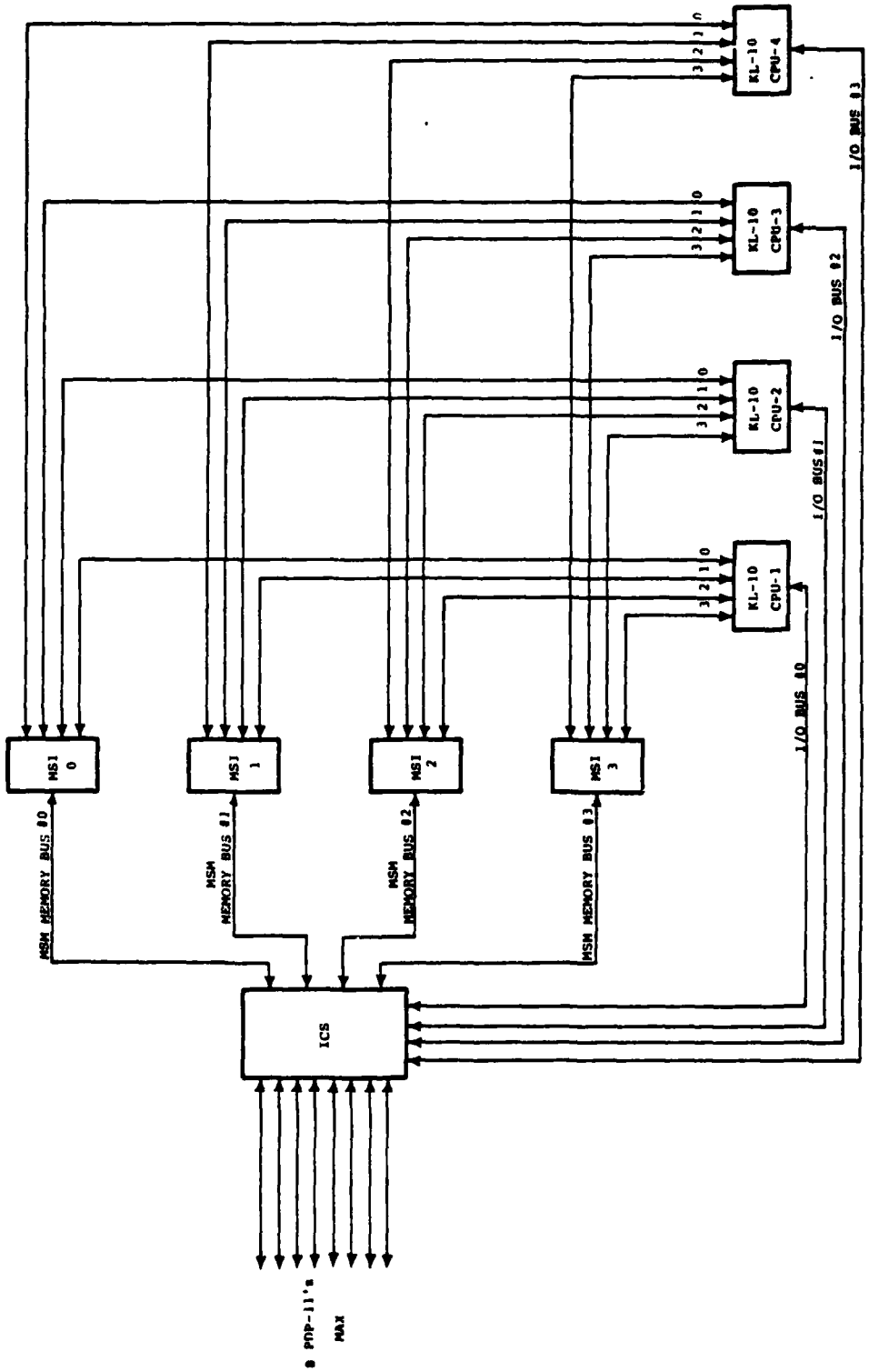

Figure 11 Four-MSI MSN Case 5

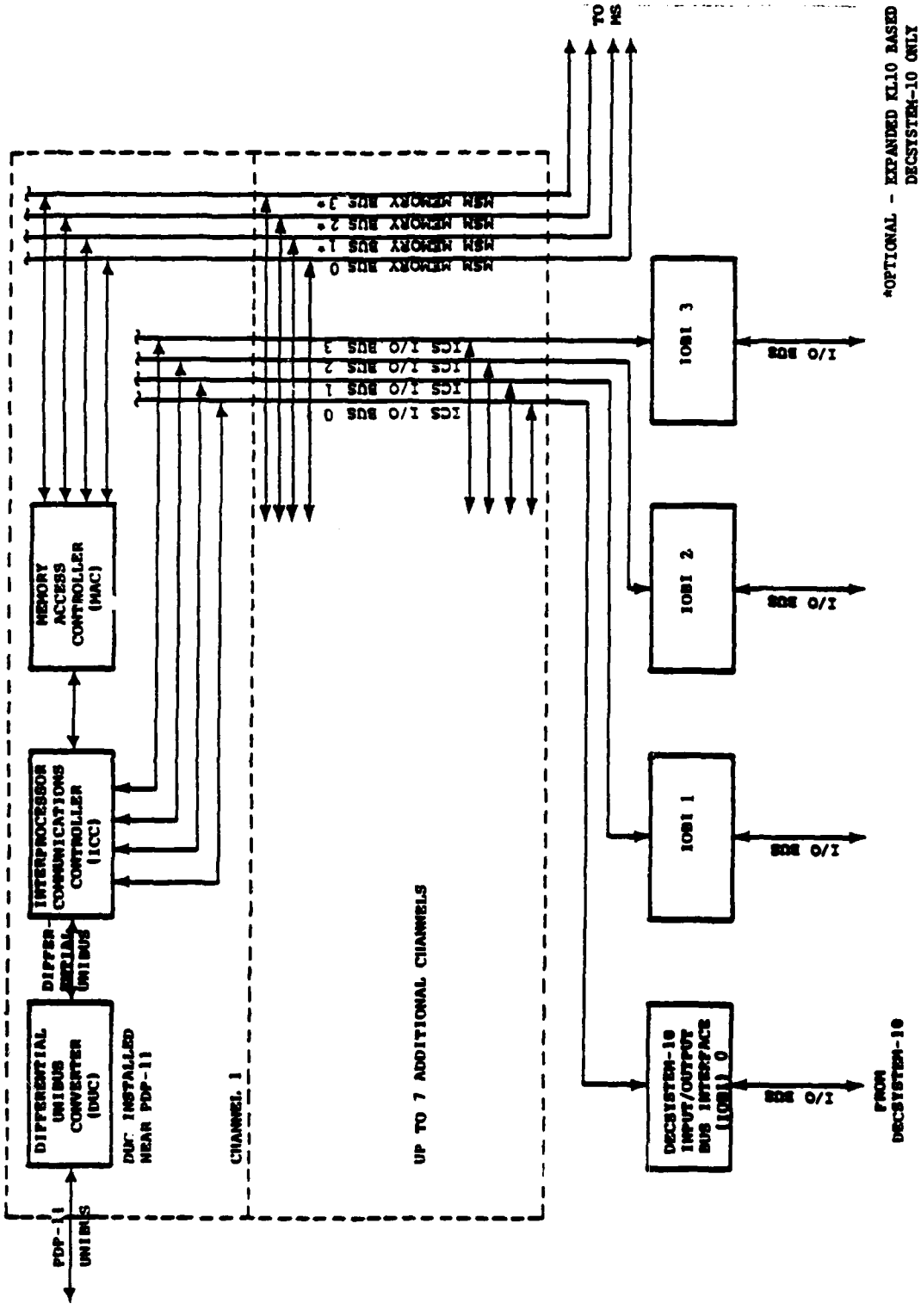

Figure 12 Interprocessor Communications Subsystem (ICS) Block Diagram

To allow PDP-11 access to memory without DEC-10 intervention, a stand-alone mode is featured with each channel. This makes it possible for a PDP-11 to access MSM memory without being under control of a DEC-10 CPU. This feature is useful for channel or SSM checkout. The stand-alone mode is determined by dip switches on one of the channel cards. It simulates a DEC-10 CPU seize and sets up certain registers including the memory mapping RAM.

Appendices I and II list the MSM registers and give detailed bit definitions for each. Some registers can be accessed by both PDP-11's and DEC-10 processors and some cannot. Some registers can only be read, others only written, and others both read and written. Some bits written by a DEC-10 CPU to a register can be read by a PDP-11 in another register and vice versa. The bits of the same register can be defined differently for data out as opposed to data in. Some bits are used as control pulses or as enables and are not actually stored. The rest of the specification refers to the registers often and the appendices will be useful as a guide.

3.2.1.3.1 DEC-10 Input/Output Bus Interface (IOBI)

The IOBI is the functional and electrical interface between the DEC-10 I/O bus and the ICS I/O Bus. The IOBI communicates with 57 DEC-10 I/O bus lines: 36 bidirectional data lines, seven device select lines, five command lines, seven priority interrupt lines, a reset line, and a strobe line used during interrupt operations. If the DEC-10 I/O bus device select lines match the device code of the IOBI, the IOBI will respond to the command lines. Device codes are switch selectable on the IOBI. Each IOBI will respond to two device codes on the DEC-10 I/O bus. Switches to select an IOBI number assignment (zero, one, two, or three) are available. When a DEC-10 user program accesses an IOBI, it must know which of the four IOBI's it has accessed. Each IOBI is located on one circuit board and is interchangeable with any other IOBI board by interchanging device codes and IOBI number assignments.

The DEC-10 I/O bus generates four different commands: Condition Out (CONO), Condition In (CONI), Data Out (DATAO), and Data In (DATAI). The IOBI performs different functions depending on which of the two device codes is selected and which of the four commands is received.

When the first device is selected, the following functions can be performed. A CONO, in conjunction with DEC-10 I/O bus data bits 18-35, can cause PDP-11 channels to be seized and released, resetting of the IOBI, and setting of the DEC-10 keep alive bit. A CONI reads MSM status conditions on DEC-10 memory bus data bits 0-35. The information received includes: PDP-11 channels seized by this CPU, channels seized by another CPU, whether MSM memory is on line, the starting address and size of MSM memory, and the IOBI number assignment. A DATAO, in

conjunction with DEC-10 memory bus data bits 0-35, can write data to registers located in a seized channel. DEC-10 memory bus data bits 5-7 are latched in the IOBI and select the PDP-11 channel. Bits 9-11, also latched, select the register. Bits 20-35 comprise the written data. Bits 0-1 are used for control. A DATAO command can also set up the PDP-11 and register select latches for a following DATAI. A DATAI reads in the contents of a previously selected register on DEC-10 I/O bus lines 20-35.

When the second device is selected, the following function can be performed. A CONI reads in interrupt status information on DEC-10 I/O bits 21-35. The information received includes which PDP-11's are interrupting on the selected PI level and on which PI levels interrupts are present. A CONO, DATAO, or DATAI command causes no IOBI activity when the second device is selected.

When the DEC-10 is interrupted by a device like the IOBI, one of the DEC-10 I/O bus priority interrupt lines PI 1-7 is asserted. The DEC-10 senses the interrupt, but does not know which device sent it. It converts the PI level to binary and transmits it to the peripheral devices as DEC-10 I/O bus bits 0-2 along with a special strobe signal (PI REQ SYNC). Each device on the I/O bus latches this value, compares it to any priority interrupt levels it has asserted, and sets a status bit indicating whether it sent the interrupt. The DEC-10 reads the status bits from each device and jumps to the interrupt service routine of the device which interrupted. If two devices are interrupting on the same level at the same time, the DEC-10 software determines which device gets priority. The IOBI has a register which latches the selected PI level and transmits it to all the seized PDP-11 channels. Each channel sends back status lines indicating whether it sent the interrupt. These lines tell which, if any, PDP-11's are interrupting on the selected PI level.

The IOBI also has tri-state drivers to send seized and interrupt status to the front panel. A block diagram of the IOBI is shown in Figure 13.

3.2.1.3.2 Interprocessor Communications Subsystem (ICS) I/O Bus

The ICS I/O Bus connects each IOBI to every channel. The ICS I/O Bus signals showing source, destination and function are listed in Table V. The ICS I/O Bus consists of 82 lines which are used as follows: 30 for seizing and releasing channels, 31 for data transfers, 19 for PDP-11 to DEC-10 interrupts, and two for CPU status.

3.2.1.3.3 Channels

One Channel serves as an interface to one PDP-11 UNIBUS, one to four ICS I/O Busses, and one or four MSM Memory Busses. A channel consists of the Differential UNIBUS Converter (DUC), the Interprocessor Communications Controller (ICC), and the Memory Access Controller (MAC). There must be one channel for each PDP-11 connected to the MSM.

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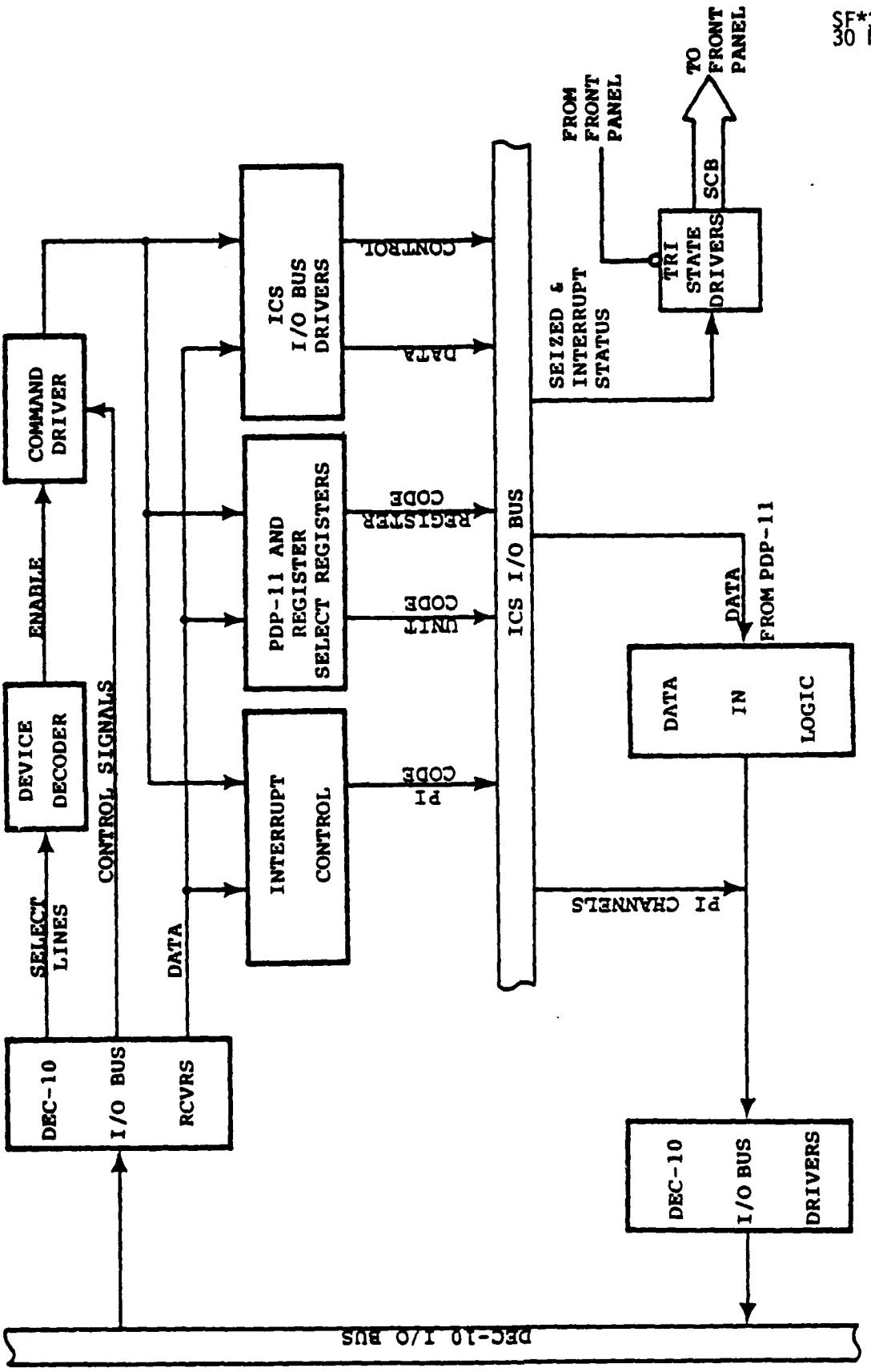

Figure 13 DEC-10 Input/Output Bus Interface (IOBI) Block Diagram

3.2.1.3.3.1 Differential UNIBUS Converter (DUC)

The DUC converts PDP-11 single ended UNIBUS signals to differential pair signals, thereby, improving noise immunity and increasing the allowable UNIBUS cable length. The DUC is installed at the PDP-11 which can be located up to 150 feet away from the rest of the MSM. The differential signals are transmitted between the DUC and ICC on individually shielded twisted pair cable. Optically coupled isolator circuits receive the differential signals at the ICC and DUC providing electrical isolation between the systems (Figure 14).

The differential data bus is bidirectional and must be properly set up for data transfer. The DUC converts and passes UNIBUS addresses, status, and control signals to the ICC which decodes them and determines whether a read or write is to occur. For the write operation, the DUC enables its data bus drivers and the ICC enables its receivers and latches the data. For a read operation, the ICC enables its drivers and sends the signal DATI to the DUC. DATI causes the DUC to enable its differential bus receivers and its UNIBUS drivers to pass the data to the PDP-11.

The DUC receives two kinds of bus requests for interrupt from the ICC. Signals BR4-BR7 are generated by a DEC-10 CPU and ERR BR is generated by an error condition in the MSM. The DUC has identical interrupt control circuits for BR4-BR7 which handshake with the UNIBUS. An ERR BR signal is sent to the PDP-11 as a BR6. The DUC has a first come, first served circuit which handles BR6 and ERR BR. If BR6 and ERROR BR arrive at the DUC at the same time, BR6 will always get priority.

When a DEC-10 CPU generates an interrupt (BR4-BR7), it also specifies the interrupt vector address. The DUC generates signals called VECSTB and AO=1 which enable the seven bit vector onto the data bus and clear the bus request. When the DUC receives an ERR BR, it generates VCESTB and AO=0 which clear the request. The error vector address is obtained from switches on the DUC.

The DUC logic is mounted on a standard PDP-11-compatible, wire-wrap board. The board is plugged into a PDP-11 peripheral mounting panel at the PDP-11. Five volt power will be provided by the PDP-11 power supplies.

3.2.1.3.3.2 Interprocessor Communications Controller (ICC)

The ICC serves as an interface to the differential UNIBUS, one to four ICS I/O Busses, and to the MAC. It contains the seize and release logic for the ICS I/O Busses; DEC-10 and PDP-11 control and status registers; function registers; bidirectional interrupt logic and front panel logic. It provides data paths to the MAC for both the PDP-11 and the ICS I/O Bus (Figure 15).

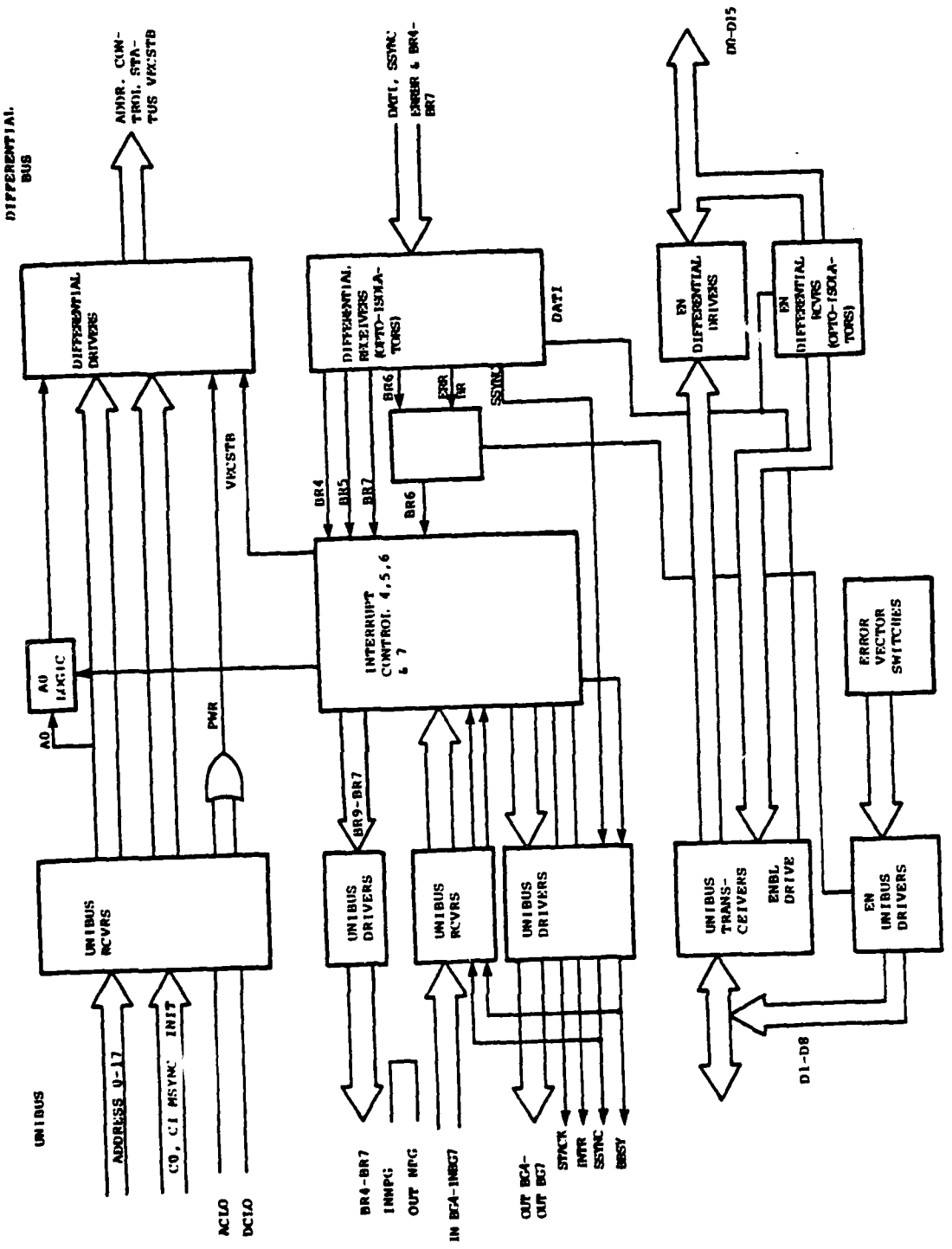

Figure 14 Differential UNIBUS Converter (DUC) Block Diagram

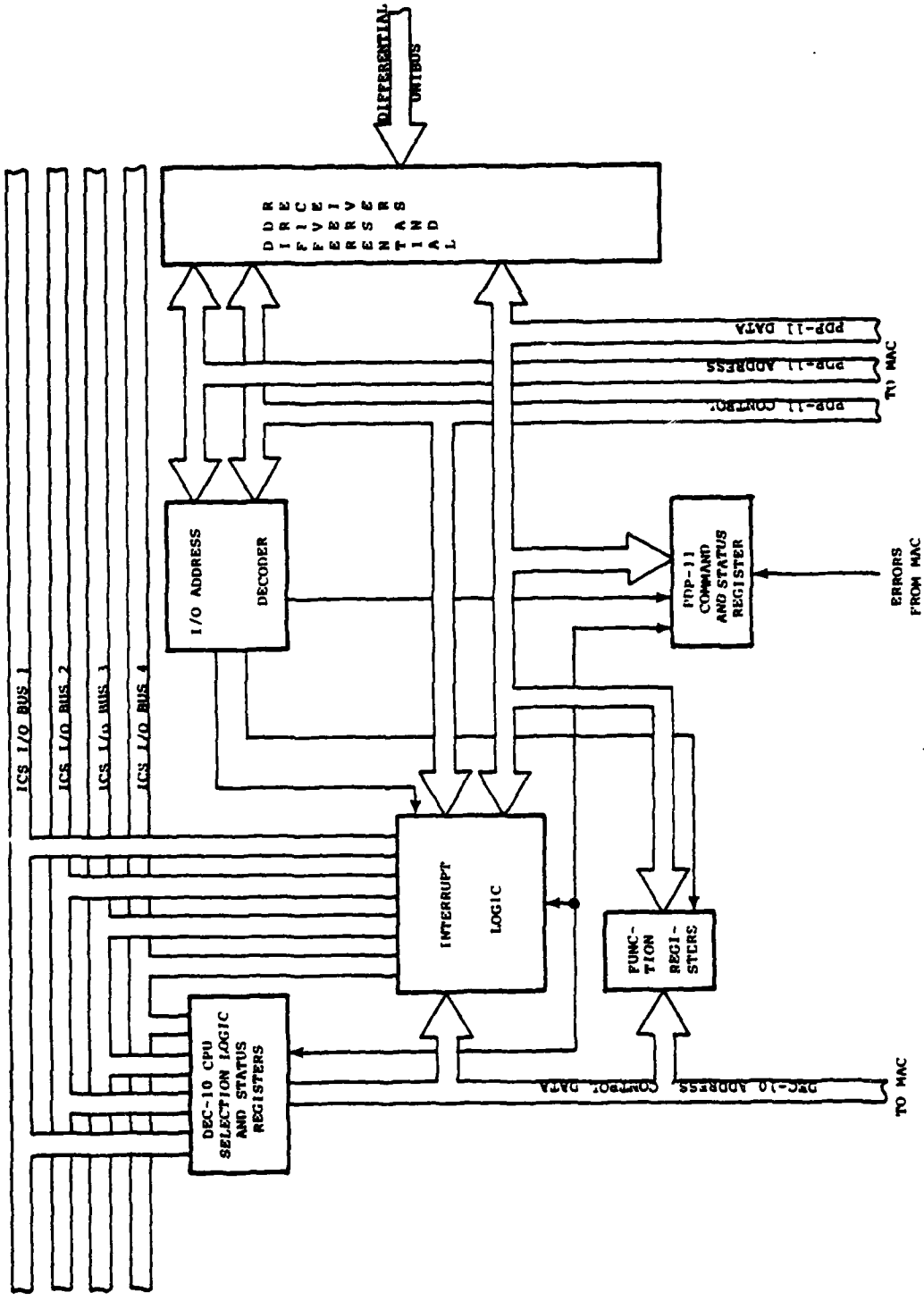

Figure 15 Interprocessor Communications Controller (ICC) Block Diagram

The ICC has differential drivers and optically coupled isolator receivers to provide the interface to the differential UNIBUS. There are six PDP-11 I/O registers in the ICC whose addresses increase consecutively in increments of two from an assigned base address. The PDP-11 I/O base address is switch-selectable. Any UNIBUS address above 760000$_8$ (248K bytes) can be used for the I/O registers base address.

The ICC has 4-1 multiplexing circuitry to allow only one ICS I/O Bus to access it at a time. Only the DEC-10 CPU which had previously seized the channel is allowed access to the ICS I/O Bus. The ICC decodes the PDP-11 number and register number and responds to ICS I/O Bus commands, if these numbers are valid.

There is one channel register which can be read by any DEC-10 CPU without first having the channel seized. This register contains status information on whether the PDP-11 is turned on and which, if any, DEC-10 CPU has the channel seized. The ICC has separate register and PDP-11 decode circuitry for each ICS I/O Bus to allow this capability.

The channel number assignment (0-7) is selected with switches on the ICC board. The board plug-in slot is prewired for a particular channel number, therefore, the switch setting must match the slot number. An ICC is located on two circuit boards which are identical to and interchangeable with any other ICC boards. A DEC-10 CPU can access 256 registers through the ICC. Eight registers, numbered 400-407 octal, are located at the ICC while 248 registers (the memory mapping RAM), numbered 0-367 octal, are located in the MAC.

Both PDP-11 and DEC-10 accessible registers in the MSM are used to enable or implement a function or to present MSM status conditions. Writing some bits to some registers causes immediate actions such as interrupts. Writing to other registers, such as memory mapping RAM, determines where the PDP-11 accesses SSM and no immediate response is received although control is implemented. There are two general purpose registers which can be read and written by both the PDP-11 and DEC-10. These registers have no effect on the MSM hardware and are intended to be used for communications.

The ICC also has front panel interface logic consisting of tri-state drivers to send channel information to the front panel and circuitry to respond to front panel switch control.

Another function of the ICC is to allow DEC-10 to PDP-11 and PDP-11 to DEC-10 interrupts. Actually the functions required to implement interrupts are shared among the DUC, ICC, and IOBI. The interrupt functions of the ICC are described in detail in the sections following.

3.2.1.3.3.2.1 DEC-10 to PDP-11 Interrupts

There are certain requirements which must be met before a DEC-10 to PDP-11 interrupt is possible. The DEC-10 CPU must have the channel seized, the PDP-11 must set its interrupt enable bit and the DEC-10 CPU must write a seven bit vector address to an ICC register. This is the address where the PDP-11 traps when an interrupt occurs.

To start the interrupt, the DEC-10 CPU writes a three bit bus request level (BR4-7) to a channel register. This three bit level is tied to a 3-8 decoder and a bus request line to the DUC is asserted. The DUC passes the bus request to the PDP-11 and provides the UNIBUS handshake signals required to gain control of the UNIBUS. The DUC sends the signals VECSTB and AO=1 to the ICC to enable the seven bit vector address into the data bus. The DUC asserts the UNIBUS INTR line, strobing the vector into the PDP-11. The PDP-11 asserts SSYNC which causes the DUC to release the UNIBUS and to negate VECSTB. The negation of VECSTB causes the ICC to clear the bus request register which removes the bus request. SSYNC is negated by the PDP-11 and the PDP-11 jumps to the interrupt routine. During this transaction, the PDP-11 interrupt enable bit is cleared.

3.2.1.3.3.2.2 Error Interrupts to the PDP-11

A parity error or a write protect error detected in the MAC will set error bits in the ICC. If the PDP-11 has enabled its error interrupt enable bit, an error bus request line will be asserted. The DUC sends an error bus request to the PDP-11 (BR6). The DUC performs the same functions as described above except it sends VECSTB and AO=0 to the ICC. The ICC clears its error bus request flip-flop on the negation of VECSTB. The DUC enables the vector address selected (with switches) at the DUC onto the UNIBUS. The PDP-11 jumps to the interrupt service routine which can read the channel register to determine which error condition caused the interrupt.

3.2.1.3.3.2.3 PDP-11 to DEC-10 Interrupts

There are certain requirements which must be met before a PDP-11 to DEC-10 interrupt is possible. The PDP-11 channel must be seized by a DEC-10 processor. The DEC-10 CPU must write one or two 3-bit priority interrupt levels on which it will accept an interrupt to an ICC register. These are called priority interrupt levels A and B. The DEC-10 CPU must set its interrupt enable bit. If the interrupt enable bit is set, any priority level is nonzero, and an interrupt request transaction is not in progress, an interrupt can be initiated.

To start the interrupt the PDP-11 must set either level A or B bits in its I/O base address register. This bit enables a 3-8 decoder whose input is the PI level and whose output is priority interrupt lines 1-7. The asserted PI line is routed to the DEC-10 CPU which has this channel seized. The DEC-10 senses the PI line, converts it to 3-bit binary code, and strobes it into the IOBI register. This PI level is sent to each channel which the DEC-10 CPU has seized. The ICC compares this

level to the PI level which it has asserted. If they match, the ICC asserts its "This PDP-11 interrupting on the selected level" line which goes to the IOBI. The DEC-10 reads these IOBI lines and determines which PDP-11 initiated the interrupt. If two PDP-11's are interrupting, the DEC-10 software determines which gets priority. The DEC-10 software jumps to the correct interrupt service routine determined by which PDP-11 is interrupting on which level. The DEC-10 software sets a bit in the channel register which clears the interrupt request. The hardware sets the level interrupt enable bit and new interrupt requests can be accommodated.

If interrupts are being requested on levels A and B at the same time, two priority interrupt lines will be asserted. The DEC-10 will respond to the lower numbered PI line first. When the DEC-10 CPU clears the interrupt request, only the level request being serviced will be cleared. The remaining PI line will remain asserted until it has been serviced. If PI levels A and B are the same, requesting on both levels will only cause one line to be asserted and both level requests will be cleared when the interrupt is serviced.

3.2.1.3.3.3 Memory Access Controller (MAC)

The MAC (Figure 16) controls the access of the PDP-11 to the MSM memory. The control is provided by the seizing DEC-10 CPU, front panel switches, and switches in the ICC. The PDP-11's address and data bits are modified by the contents of DEC-10 written registers and the switch settings. The MAC has demultiplexing and handshake logic to interface with four MSM Memory Busses.

Before the PDP-11 can start accessing the SSM its channel must be initialized. The initialization is done by the DEC-10 and consists of writing page map and control information to the memory mapping RAM in the MAC and page limit and address mode information to an ICC register. Switches in the ICC are used to select the desired 4K boundary base address. The interleave switch, on the front panel, must be correctly positioned. All this information is used by the MAC for address calculations.

The operation of the MAC is based on the organization of the SSM. The SSM is organized into 512 word pages. Each SSM word is 40 bits long. Because a PDP-11 word is only 16 bits long, two PDP-11 words can be stored in one SSM. The PDP-11 data stored in the SSM word is determined by address mode bit (1-1 or 2-1). In 1-1 mode, a page consists of 512 words. In 2-1 mode, a page consists of 1024 words. The memory mapping RAM relocates PDP-11 pages in the SSM. The SSM has up to 128K of memory in each MSI module or 512K for a four MSI module system. Memory of 512K is equivalent to 1024 SSM pages. There are ten address translation bits in the memory mapping RAM to relocate any PDP-11 page to one of 1024 SSM pages.

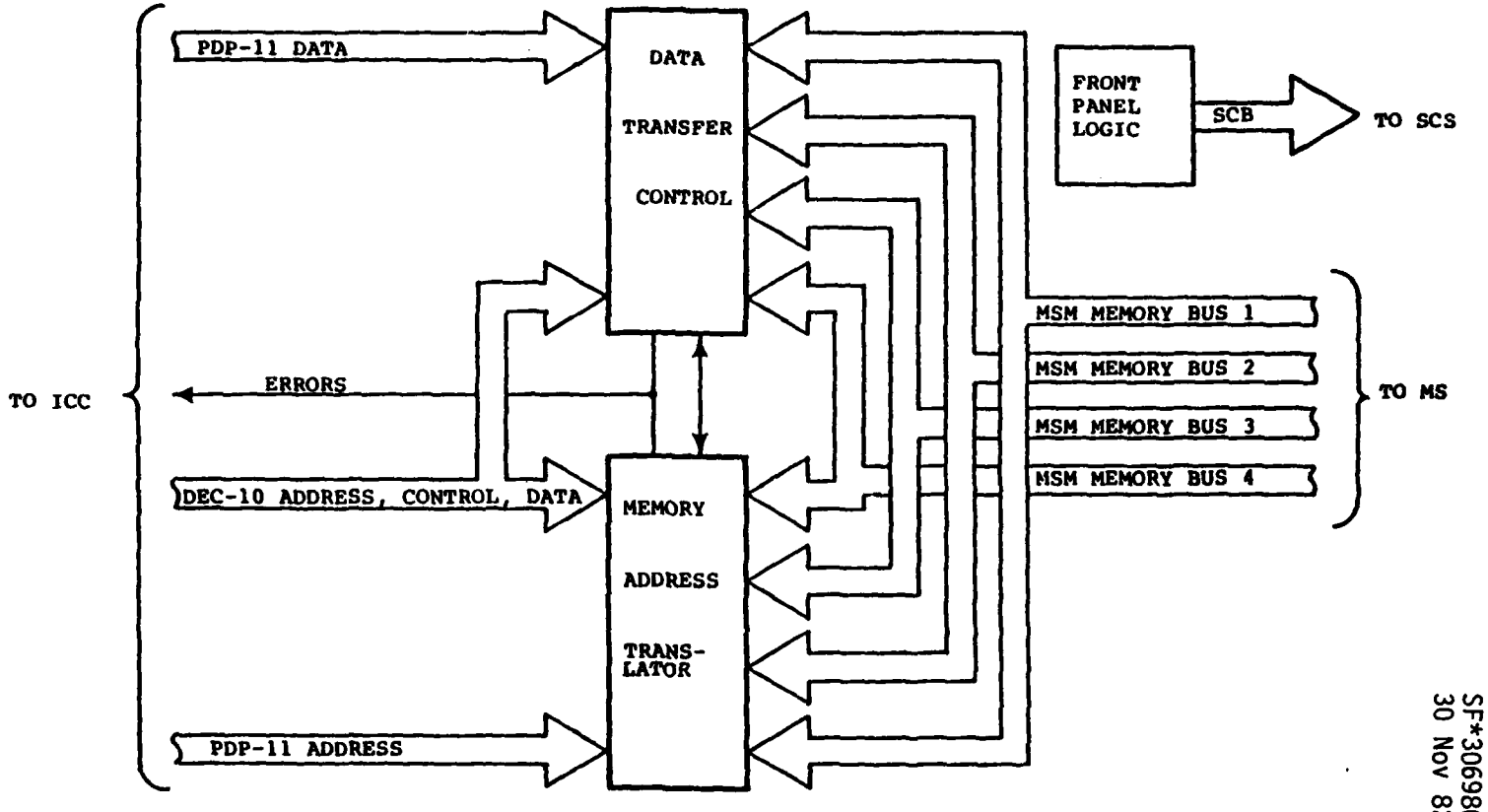

Figure 16 Memory Access Controller (MAC) Block Diagram

The PDP-11 address is 18 bits long and can access 256K bytes or 128K 16-bit words. The upper 4K of the PDP-11 addressing is allocated for I/O, leaving 124K memory addressing capability. The PDP-11 address is checked in the ICS I/O Bus to determine if less than 124K. In the MAC, the 4K boundary base address is subtracted from the PDP-11 address to obtain an 18-bit net address. If the PDP-11 address is less than the 4K boundary, SSM access will not occur. The net address runs into a 2-1 multiplexer which shifts the address right one bit, in 2-1 mode; in 1-1 mode, it has no effect. Shifting the address is equivalent to dividing by two. The 19-bit output of this multiplexer is divided into two groups consisting of eleven lower bits and eight upper PDP-11 page bits. The PDP-11 page bits are compared with the "upper page limit" value and must be less than this value. The PDP-11 page bits are input to the memory mapping RAM which outputs a 13-bit data word. Three data bits are for page control and ten are for address translation. The ten address translator bits (from the memory mapping RAM) and eleven lower addressing bits are run into a 2-1 multiplexer which shifts them two bits right if in interleaved mode and has no effect otherwise. Shifting two bits right is equivalent to dividing by four. The 21-bit output of this multiplexer consists of 17 SSM compatible address bits, two MSI modules select bits, one word and one byte select bit. Use of the PDP-11 address bits for the different memory addressing modes is summarized in Table VI.

The three page control bits in the memory mapping RAM are invalid page, write protected page, and sign extend. If the invalid page bit is set, the MAC will not access the SSM and will not return SSYNC to the PDP-11. The PDP-11 will time out and assume non-existent memory for this page. If the write protected page bit is set and the PDP-11 is attempting to write, the MAC will not access SSM but it will return SSYNC. The MAC will set the write protect violation error flag in the PDP-11 status register in the ICC so the user can detect the error. The PDP-11 can read a write protected page. The sign extend bit is routed to the data conditioner section of the MAC.

To allow PDP-11 byte manipulation, the data conditioner receives the PDP-11 byte or word and converts it to 40 bits. First, odd parity bits are generated for each data byte and the resulting 18 bits are latched by MSYNC. For a byte write, the eight unused bits are latched in the logic one state.

The output of these latches are run into a 4-1 multiplexer which alters the data based on the address mode (2-1 or 1-1) and the sign extend bit for this page. In 2-1 mode, the 18 data and two parity bits are put on the upper and lower halves of the data bus and in 1-1 mode they are put only on the lower half. The extra bits in either address mode are filled with zeros if the sign extend bit is zero. The most significant bit is extended into the extra bits if the sign extend bit is a one. The resulting 40 bits are transmitted to the SSM.

For a read operation, twenty bits of data are received from the SSM. The data is split into groups of nine bits and eleven bits and odd parity is checked on each group. If a parity error is detected, a "parity error" flag is set in the PDP-11 status register in the ICC so the user can detect the error.

If the PDP-11 address is within the MSM memory range, MSYNC will cause the MAC to request SSM access from one of four MSI modules. There are seven control lines sent to the MAS which determine SSM access. These are defined in Table I. During a SSM fetch operation only parts of a SSM word will be read or written. The signals that strobe the SSM are defined in Table II as part of the SSM Bus. Table III lists the SSM access modes and Figure 3 illustrates how the strobe signals control the SSM.

For PDP-11 access to MSM memory without DEC-10 CPU control, a stand-alone mode is featured. This channel feature located on the MAC simulates a DEC-10 CPU seize and sets up the memory mapping RAM and page limit/address mode register. It is implemented by a set of dip switches on one of the MAC cards. It is useful for the check out of a channel without the need of a DEC-10.

The MAC has tri-state drivers to interface to the SCS. The MAC is located on two circuit boards which are interchangeable with any other MAC boards.

3.2.1.4 Status and Control Subsystem (SCS)

The SCS consists of the Status and Control Bus, Memory Status and Front Panel Logic (MSFPL) card, and the Front Panel. The Status and Control Bus transfers status and control signals among the SSM, the Front Panel, and MSFPL. The Front Panel is mounted to the cabinet for easy operator access. The MSFPL is mounted to the back of the Front Panel.

3.2.1.4.1 Front Panel

The Front Panel (Figure 17) consists of displays, switches, and dials to allow an operator to control and monitor the MSM. The Front Panel is divided into five monitor sections and two control sections. Four monitor sections have dials to select a particular module and the displays indicate the status of that module. The fifth error monitor section displays system errors. All indicators are discrete (one indicator for one condition or module) unless otherwise indicated. One control section consists of the total MSM control switches. The other control section contains the power control switches.

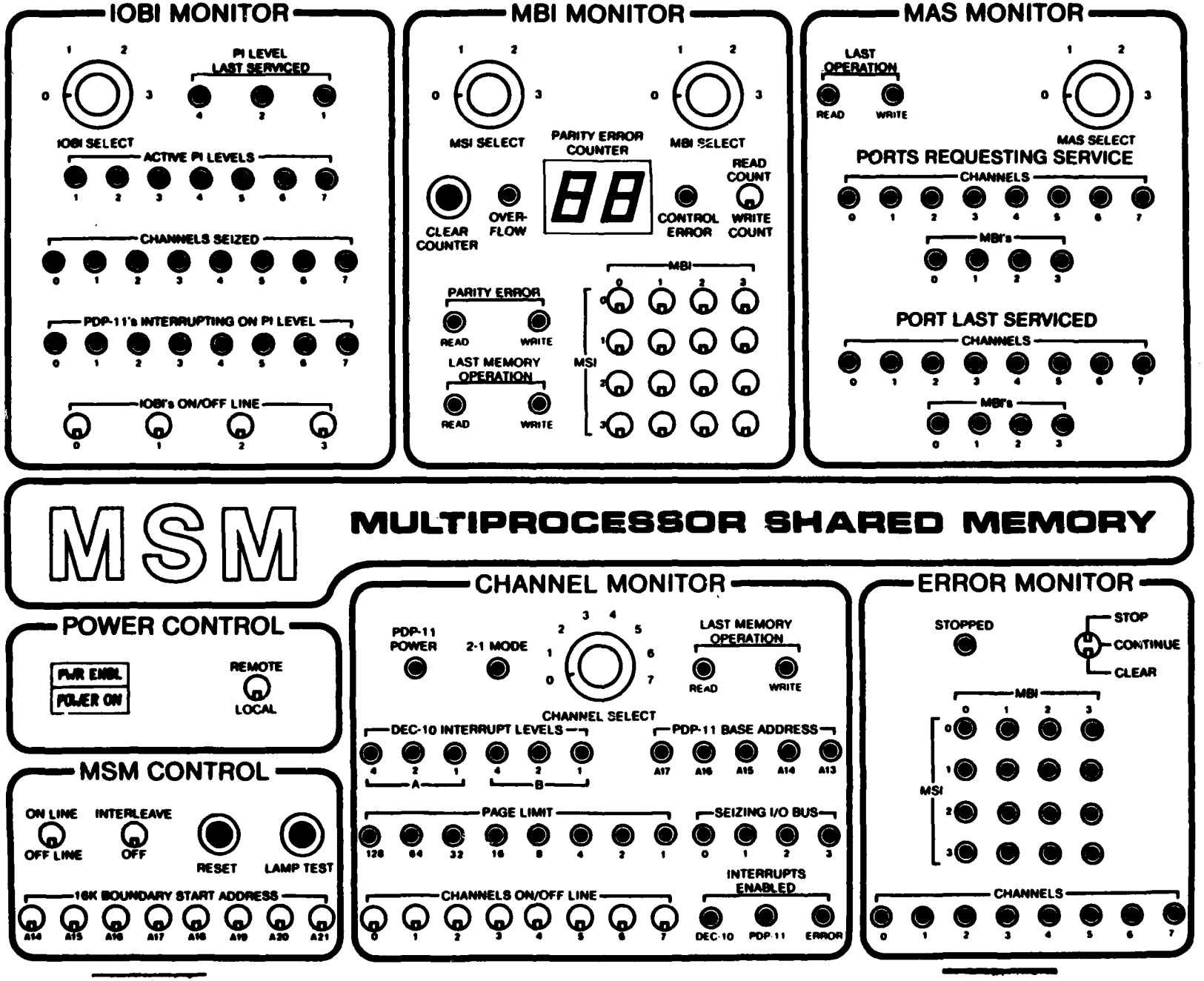

Figure 17 Front Panel

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3.2.1.4.1.1 Power Control Section

This section consists of a POWER ON/OFF switch and a REMOTE/LOCAL switch. In local mode, power is turned on at the Front Panel. In remote mode, power turn on is enabled at the Front Panel and implemented by the DEC-10. In either mode, power can be turned off at the Front Panel.

3.2.1.4.1.2 System Control Section

The switches of this section effect the total MSM system. The MSM ON/OFF LINE switch causes the IOBI's, DUC's, and MBI's to fail to respond to bus commands, if in the off line position. Pressing the LAMP TEST button causes all the front panel indicators and segments to light. The INTERLEAVE switch in the up position causes the MSM memory to be four-way interleaved. The DEC-10 memory busses and the MSM must be specially configured for interleaving. The 16K BOUNDARY START ADDRESS switches allow the operator to select the start address for MSM memory in the DEC-10 memory space. The MSM RESET switch terminates any operation in progress and returns all MSM flip-flops to the power-up condition.

3.2.1.4.1.3 IOBI Monitor

The CHANNELS SEIZED lights indicate which of eight channels this I/O Bus Interface has seized as selected by the IOBI SELECT dial. The ACTIVE PI LEVELS lights indicate which of seven priority interrupts of the IOBI is being requested. The PI LEVEL LAST SERVICED lights indicate which of seven priority levels was last serviced by the IOBI. These lights are read as binary and weighted 4-2-1 left to right. The PDP-11's INTERRUPTING ON PI LEVEL lights indicate which of the eight PDP-11's are interrupting on the priority interrupt level last serviced. The IOBI ON/OFF LINE switches cause an IOBI to fail to respond to I/O bus commands, if in the off line position.

3.2.1.4.1.4 MBI Monitor

As in all monitor sections, the MBI of interest is selected by using dials. The MBI SELECT dial, used in conjunction with the MSI SELECT dial, gives the capability to monitor one of sixteen MBI's from four MSI modules configured for interleaving. In addition, there is a parity error count display that indicates either read or write parity errors as selected with the dials. The PARITY ERROR COUNTER can display from 0-99. If the counter has overflowed, the OVERFLOW light illuminates. Depressing the CLEAR button clears only the selected counter. The read and write PARITY ERROR and CONTROL ERROR lamps indicate the error history. A control error occurs when a DEC-10 read-modify-write construction fails to terminate within 25us. The READ and WRITE lamps indicate the last memory operation occurred. There are discrete on/off line switches for each MBI/MSI which make a MBI unresponsive to the DEC-10 memory bus when in the off line position.

3.2.1.4.1.5 MAS Monitor

The PORTS REQUESTING SERVICE lamps indicate which channels or MBI's are currently requesting service. The PORT LAST SERVICED lights indicate which port was last serviced. The WRITE and READ lamps indicate the last operation. If both are lit, a read-modify-write operation occurred. The MAS SELECT dial allows monitoring of each MAS located in MSI 0-3, if MSM is in a four-way interleave mode.

3.2.1.4.1.6 Channel Monitor

The INTERRUPTS lamps indicate if the selected channel has its interrupt modes enabled. The DEC-10 INTERRUPT LEVELS lamps are read as binary and weighted 4-2-1 (left to right) for level A and B. The SEIZING I/O BUS lamps indicate which of four I/O busses has this channel seized. The PAGE LIMIT lamps indicate the last page in the MSM memory which is accessible to this channel. The PDP-11 BASE ADDRESS lamps indicate the PDP-11 4K boundary where the MSM address space starts. Both page limit and base address lamps are read left to right as binary numbers. The LAST MEMORY OPERATION lamps indicate whether the last operation was a read or a write. The PDP-11 POWER lamp indicates whether the PDP-11 connected to this channel is turned on. The CHANNELS ON/OFF LINE switches cause the channel to ignore UNIBUS commands when in the off line position.

3.2.1.4.1.7 Error Monitor

The STOP-CONT-CLEAR switch causes the MSM to halt on the next error if in the stop position. In the CONT position, the MSM will continue running regardless of errors. The clear position is momentary contact and clears all error flip-flops in every channel and MBI. The STOPPED lamp indicates the MSM is in a stopped condition due to the STOP-CONT-CLEAR switch being in the STOP position and an error occurring. The MBI lamps indicate an error has occurred in the MBI. To determine the type of error, the MBI in the monitor must be used. The CHANNELS 0-7 lamps indicate a read parity error has occurred in a channel.

3.2.2 Physical Characteristics

The physical characteristics of the MSM depend on final system configuration (number of PDP-11 channels, number of MSI's, size of memory, etc.). The maximum MSM configuration (eight channels, four MSI's, sixteen DEC-10 memory bus connections, 512K memory) shall not require more than four standard equipment cabinets, each housing two MSM card racks.

3.2.2.1 Size

The exterior dimensions of each cabinet shall not exceed 80 in. tall by 26 in. deep by 25 in. wide.

3.2.2.2 Weight

The weight of each cabinet shall not exceed 500 lbs.

3.2.2.3 Power Requirements

All power supplies shall require 115 VAC 60 Hz single phase power. Each MSM card cage shall not require more than 500 watts. Power supplies to each card cage shall provide:

+5 VDC (±10%) @ 75 amps, 30·C
-5 VDC (±10%) @ 10 amps, 30·C

3.2.3 Reliability

To Be Determined

3.2.4 Maintainability

Preventive maintenance of the MSM shall consist of a monthly visual inspection of all components including cables and connections. Performance of this task as well as any corrective maintenance requires personnel qualified at the technician or higher level.

3.2.5 Environmental Conditions

The MSM shall be capable of oeprating in the same laboratory environment as the PDP-11 minicomputer and exceeds that of the DECsystem-10. These conditions are defined in the PDP-11 Peripherals Handbook.

3.3 Design and Construction

The design and construction of the MSM shall follow standard commercial practices as approved by the procuring activity.

3.3.1 Material, Processes, and Parts

The MSM will be constructed using standard commercial grade components.

3.3.2 Electromagnetic Radiation

No signals produced by the MSM shall interfere with or be affected by other equipment operating in the simulation laboratory environment as defined in 3.2.5. Circuitry grounding paths shall be controlled to minimize the interaction of ground currents with other circuits which are either internal or external to the MSM.

3.3.3 Identification and Marking

Nameplates and identifications shall be in accordance with the requirements of MIL-STD-130. When the item is too small to accommodate a nameplate, it will be identified by permanent type marking applied to the part using any suitable means authorized by MIL-STD-130.

3.3.4 Workmanship

All operations shall be controlled by the manufacturer's process specifications and standards to ensure that the engineering quality, safety and reliability requirements of the equipment are achieved. Workmanship shall be in accordance with MIL-STD-454E, requirement 9 and subject to inspection and approval of the cognizant inspection activity.

3.3.5 Interchangeability

Other than the circuit cards mentioned in this specification, the interchangeable MSM items include DEC-10 bus cables and common integrated circuit types.

3.3.6 Safety

The MSM shall be constructed utilizing techniques that minimize hazards to operating and maintenance personnel. These techniques shall be in accordance with MIL-STD-454E, requirement 1.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

All tests described in this section assume that the user has a minimum of one PDP-11 and one DECsystem-10 connected to the MSM system.

4.1.1 Responsibility for Inspection

The responsibility for performing all specified test/verifications rests with the supplier. The customer may reserve the right to witness or seperately perform all tests specified or otherwise inspect any or all tests and inspections.

4.1.2 Special Tests and Examinations

The operation of the MSM system may be fully tested and verified using simple hardware test points and software diagnostics.

4.1.2.1 Installation

Before the system is initally used the following test should be done:

- o Before plugging MSM to a power source:
- o Remove all cards from backplane.
- o Do not connect DECsystem-10 and PDP-11 to system.
- o Verify the power source that is to be used meets the power requirements outlined in section 3.2.2.3.
- o Plug MSM power cord to the selected power source. Turn Front Panel Power Switch on.
- o Verify that all voltages are correct on the backplane (Refer to the Drawing Package for proper pinouts and voltage locations).

- o Turn Front Panel Power Switch off.
- o Unplug MSM power cord from its power source.
- o Plug all delivered MSM cards into the appropriate slots in the backplane (Refer to the Drawing Package for proper board identifications and locations).
- o After all boards have been properly seated and their locations have been verified, plug MSM power cord back into the power source.
- o Turn Front Panel Power Switch on.
- o Once again, verify that all voltages are correct on the backplane.
- o Turn Front Panel Power Switch off.
- o If any of the previous tests has failed, check the power supplies or the backplane wiring.
- o At this time the MSM can be connected to the DECsystem-10 and PDP-11.
- o Connect the DECsystem-10 memory bus(es) to the MSM. Keep in mind that if the MSM is the last unit in the memory bus chain the output (bypass) memory connector must be terminated.
- o Connect the DECsystem-10 I/O bus(es) to the MSM. Keep in mind that if the MSM is the last unit in the I/O bus chain the output (bypass) I/O Connector must be terminated.
- o Connect the PDP-11 DUC(s) to the appropriate PDP-11 UNIBUS(s).
- o The PDP-11 base address should now be configured in the appropriate ICC. The address selection should be coordinated with the PDP-11 support group and then documented for future reference.

4.1.2.2 Memory Tests (Non-PDP-11 Interactive)

The tests that fall under the section of "Memory Tests" will allow a user to fully exercise the MS. All tests should be run repetitively to allow possible intermittent failures to be found.

4.1.2.2.1 Zero Test

This test will ensure that all MSM memory can be cleared. Every word within MSM memory will be individually set to zero and then read to verify that all bits can be set to zero.

4.1.2.2.2 Ones Test

This test will ensure that all MSM memory can be set. Every word within MSM memory will be individually set to ones and then read to verify that all bits can be set to ones.

4.1.2.2.3 Address Test

This test will ensure that each MSM memory word can be uniquely addressed. Every word within MSM memory will be individually set to its relative address. After all words have been written the diagnostic will read the memory and verify that all words have the original data.

4.1.2.2.4 Dual Addressing Test

This test is the most comprehensive of the memory tests. The dual addressing test will verify that each bit in every word is uniquely addressable. This ensures the integrity of the MS decoders.

All of the available MSM memory is first set to zeros. The first MSM word is then set to all ones. Every MSM word other than that set to all ones is checked to verify that its contents are zero. If the word is non-zero, the diagnostic will determine whether it was a dual-addressing high or low error and report it to the user. If no errors exist the first word will be reset to all zeros and the second word will be set to all ones. This test will be repeated for every word within MSM memory.

4.1.2.3 I/O Port Register Tests (Non-PDP-11 Interactive)

The tests that fall under this category will allow a user to exercise all internal registers that do not require PDP-11 interactions. (Refer to Appendices I & II for a description of internal registers).

4.1.2.3.1 Seizing Hardware

This test will verify that the PDP-11's can be seized by the DEC-10 processors. This is accomplished by first seizing all PDP-11's and reading the seized register to determine how many PDP-11's are available. Next each PDP-11 will be individually seized and released. If this test fails for any PDP-11 the user will be notified.

4.1.2.3.2 Memory Mapping RAM

The memory mapping RAM will be tested in the same manner as the MSM memory. Refer to the Memory Test section of this specification for a description of the zero test, ones test, address test, and the dual-addressing test.

4.1.2.3.3 Page Limit Register

This test will ensure that the page limit register can be set to all zeros and all ones.

4.1.2.3.4 Function Registers

The two function registers will be verified for data integrity and addressability by using the ones test, zeros test, and the address test.

***Note

All of the aforementioned tests must be run error free on the MSM system before progressing to the next set of diagnostics.

4.1.2.4 Interactive Diagnostics

The following tests will require both the DECsystem-10 and PDP-11 to be connected to the MSM system.

4.1.2.4.1 Function Register Test

This test will ensure that the DECsystem-10 can communicate with the PDP-11's via the function register. This is accomplished by the DECsystem-10 writing data into one register. The PDP-11 reads the data and writes it into the other register; the DECsystem-10 then verifies the data and writes a new bit pattern in the register.

Initially the program will ask the user to input a test bit pattern; this bit pattern will be shifted to the left one bit after every pass. If the pattern finally equals zero the test will be terminated.

4.1.2.4.2 Interrupts Test #1

This test ensures that the PDP-11 can properly interrupt the DECsystem-10.

The DECsystem-10 will set-up the A&B PI channel for the PDP-11 and then enables PDP-11 interrupts to the DECsystem-10. The DECsystem-10 will place either a 1 or 2 in function register #1. The PDP-11 should then interrupt the DECsystem-10 on the appropriate channel (1=A, 2=B). This test will loop several times using various PI channels.

4.1.2.4.3 Interrupts Test #2

This test will ensure that the DECsystem-10 can properly interrupt the PDP-11. The DECsystem-10 will set both function registers to zero and then wait for function register #1 to become non-zero. The DECsystem-10 will check to see if the PDP-11 has enabled itself for interrupts. If so the DECsystem-10 will interrupt the PDP-11 after the interrupt has been processed by the PDP-11. It will set its interrupted address location in function register #2. The DECsystem-10 will verify that the correct address has been returned. This test will be repeated several times.

4.1.2.4.4 Memory Transfer

This test is the most comprehensive of all the MSM diagnostics; it exercises both the interrupt facility and the MS.

This test will have the DECsystem-10 set up the MSM for a memory transfer. Each word of the memory will contain it's relative address. The DECsystem-10 will interrupt the PDP-11, the PDP-11 will service the interrupt by adding one to the memory data and then interrupt the DECsystem-10. The DECsystem-10 will verify the data, subtract one from the data, and then interrupt the PDP-11.

This sequence will be executed approximately ten times. The 2-1 and 1-1 modes will be tested with this diagnostic.

4.1.2.5 General Tests

4.1.2.5.1 General Register Test

This test will ask the user for a register number and then for a bit pattern. The bit pattern will be written to the register and then read back and displayed to the user.

4.1.2.5.2 Non-Existent Memory Test

To ensure the integrity of DECsystem-10 memory, this test will request the PDP-11 to write to a non-valid memory location. The PDP-11 will communicate whether the read/write was successful. This will be done via the function register and interrupt facility.

4.1.2.6 Front Panel/Diagnostics

The Front Panel has been designed to allow a user to readily identify the status of the MSM system, and possibly reconfigure the system.

- o Error Monitor

  This section indicates any memory bus indicator or channel errors. The switch in this section allows a user to clear errors or specify whether the MSM is to stop or continue upon the receipt of an error.

o MBI Monitor

This section allows the user to determine if any parity read/write errors have occured. The user can examine any MBI to determine how many errors have occurred in that section.

o MAS Monitor

This section of the Front Panel indicates the status of the MS and memory port scanner.

o IOBI Monitor

The IOBI monitor reflects the status of each I/O Bus Interface. The user may specify which IOBI is to be monitored via a front panel rotary switch.

As previously discussed, the Front Panel allows monitoring (and to some degree, control) of the MSM subsystems. Some of these indicators are directly affected by the diagnostic tests described above. Table VII shows a correlation between the diagnostic tests and the front panel lights and indicators that are affected.

4.2 Quality Conformance Inspection

Confirmation that the MSM, as fabricated and assembled, complies with the requirements set forth in this specification shall be made by combinations of visual examinations and diagnostic tests. A visual inspection and comparison with the MSM configuration drawings should be made to verify that all components are present. This inspection will also allow verification of compliance with the requirements set forth in Section 3.3 of this specification. Upon successful completion of this inspection, the MSM may be installed following the procedure outlined in 4.1.2.1. Further test and verification requires use of the diagnostics. The Verification Cross Reference Index (Table VIII), shows the correlation between the diagnostic tests and the requirements set forth in Section 3.0 of this specification. Final verification of the entire MSM system can be made using the interactive memory transfer test described in 4.1.2.4.4.

5.0 PREPARATION FOR DELIVERY

The MSM shall be packaged for delivery by whatever means deemed appropriate by the manufacturer, subject to approval by the procuring activity.

6.0 NOTES

6.1 Purpose

The MSM has been designed to meet the requirements of the Avionics Laboratory at Wright Patterson Air Force Base. A device is required to allow a DECsystem-10 to communicate with one or more PDP-11's. The communications are normally the result of a real-time aircraft simulation updating a common window in DECsystem-10 memory. The PDP-11's require the data to drive graphics systems or other simulation support hardware.

6.1.1 DMA10 Replacement

Digital Equipment Corporation produced a device called a DMA10.

The DMA10 is a programmable word transfer link which interfaces one DECsystem-10 to up to eight PDP-11's. It uses a circular scanner as a means of memory request processing.

The DMA10 utilizes DECsystem-10 memory and can be configured anywhere within the lower 256K addressing space. Each PDP-11 may have up to 24K of this window.

The main limitations of this system have been its speed and the fact that all programs using the device must be locked within the first 256K of DECsystem-10 memory. (For further details refer to the DMA10 Maintenance Manual.)

6.1.1.1 Memory Priority Access (MPA)

Initial attempts to define a replacement for the DMA10 produced a development specification for a device called MPA. The MPA proposed a priority encoder scheme which was expected to greatly improve the throughput over the circular scanner method. After detailed timing was considered it was found that a PDP-11 memory access would not really be any faster than that of the DMA10. This system also used DECsystem-10 memory.

The MPA had additional drawbacks because of the functional hardware partitioning. The PDP-11 channel logic was quite complex, significantly affecting system cost as PDP-11's were added.

6.1.1.2 MSM

The MSM system incorporates internal memory using 35ns memory chips; it does not require external DECsystem-10 memory and can be configured anywhere within the four million word addressing space of the DECsystem-10.

The PDP-11 can address up to 124K of MSM memory as its own. This allows a PDP-11 to have a window as large as its full addressing space.

6.1.2 Communications/Centralized Control

A DECsystem-10 user may control from one to eight PDP-11's via the MSM system.

To use the system the following sequence of decisions and actions must be made:

- o Determine which PDP-11 is to be controlled.
  Seize appropriate PDP-11's (verify PDP-11 power on).

- o Determine whether the PDP-11 will require the DECsystem-10 interrupt facility.
  Enable appropriate Interrupt Levels (A or B).

- o Determine which of the user's pages are to be mapped within the MSM memory system.
  Map MSM pages into user page map page.
  Setup memory mapping RAM.
  Setup page limit register.
  Setup addressing mode.

- o Determine whether PDP-11 is to be interrupted.
  Setup PDP-11 interrupt address register.
  Setup PDP-11 BR register.

The MSM is now enabled for memory transfers and general use. The MSM registers that are accessable from the DEC-10 are summarized and defined in Appendix I. Appendix II summarizes the PDP-11 accessable registers.

TABLE I. MSM Memory Bus (Control Signals from Ports to MAS)

MSM MEMORY BUS	SIGNAL DESCRIPTION
MEM REQ 0-MEM REQ 11	requests from a PDP-11 or DEC-10 port for SSM access; high = false, low = true
GRANT 0 - GRANT 11	MAS grant to a PDP-11 or DEC-10 port to signify that the MEM REQ has been received high = false, low = true
GRANT SYNC	returned from PDP-11 or DEC-10 port signifying that the GRANT has been received high = false, low = true
TYPE	low = PDP-11 port request, high = DEC-10 port request
ADDRESS MODE	low = 1-1, high = 2-1 (TYPE = low only)
WORD SEL	low = lower half, high = upper half (MODE high only)
BYTE MODE	low = DATOB, high = DATO (TYPE low only)
BYTE SEL	low = lower byte, high = upper byte (BYTE low only)
DATA LATCH	strobes data into PDP-11 or DEC-10 port buffer, active low
READ	from PDP-11 or DEC-10 port, low asserted
WRITE	from PDP-11 or DEC-10 port, low asserted

TABLE II. SSM Bus (Control Signals from MAS to SSM)

SSM BUS	SIGNAL DESCRIPTION
$\overline{WRO}$	Writes MSM Memory Bus bits 28-35 and PA in SSM
$\overline{WR1}$	Writes MSM Memory Bus bits 18-27 and PB in the SSM
$\overline{WR2}$	Writes MSM Memory Bus bits 10-17 and PC in the SSM
$\overline{WR3}$	Writes MSM Memory Bus bits 0-9 and PD in the SSM
LUWD	Enables SSM data bits 18-35 and PA and PB to drive the MSM Memory Bus data lines 18-35 and PA and PB
$\overline{RDST1}$	Enables SSM data bits 0-17 and PC and PD to drive the MSM Memory Bus data lines 18-35 and PA and PB
$\overline{RDST2}$	Enables SSM data bits 0-17 and PC and PD to drive the MSM Memory Bus data lines 0-17 and PC and PD
$\overline{CS}$	Chip select - enable 2147H RAMS, when Hi, RAMS are in power standby mode

TABLE III. SSM Access Modes

PORT	FUNCTION	WORD MODE	WHICH WORD ?	WHICH BYTE ?	LOCATION (Refer to Figure 18)
PDP-11	DATA OUT	1-1	LOWER	-	A,B
PDP-11	DATA IN	1-1	LOWER	-	A,B
PDP-11	DATA OUT	2-1	LOWER	-	A,B
PDP-11	DATA OUT	2-1	UPPER	-	C,D
PDP-11	DATA IN	2-1	LOWER	-	A,B
PDP-11	DATA IN	2-1	UPPER	-	C,D
PDP-11	DATA OUT BYTE	1-1	LOWER	LOWER	A
PDP-11	DATA OUT BYTE	1-1	LOWER	UPPER	B
PDP-11	DATA OUT BYTE	2-1	LOWER	LOWER	A
PDP-11	DATA OUT BYTE	2-1	LOWER	UPPER	B
PDP-11	DATA OUT BYTE	2-1	UPPER	LOWER	C
PDP-11	DATA OUT BYTE	2-1	UPPER	UPPER	D
DEC-10	WRITE	-	-	-	
DEC-10	READ	-	-	-	
DEC-10	READ-MODIFY-WRITE	-	-	-	

TABLE IV. MSM Memory Bus Signals

SIGNAL(S)	SOURCE	DESTINATION	UNIDIRECTIONAL?
REQUEST 0	CHANNEL 0	MAS	YES
REQUEST 1	CHANNEL 1	MAS	YES
REQUEST 2	CHANNEL 2	MAS	YES
REQUEST 3	CHANNEL 3	MAS	YES
REQUEST 4	CHANNEL 4	MAS	YES
REQUEST 5	CHANNEL 5	MAS	YES
REQUEST 6	CHANNEL 6	MAS	YES
REQUEST 7	CHANNEL 7	MAS	YES
REQUEST 8	MBI 0	MAS	YES
REQUEST 9	MBI 1	MAS	YES
REQUEST 10	MBI 2	MAS	YES
REQUEST 11	MBI 3	MAS	YES
GRANT 0	MAS	CHANNEL 0	YES
GRANT 1	MAS	CHANNEL 1	YES
GRANT 2	MAS	CHANNEL 2	YES
GRANT 3	MAS	CHANNEL 3	YES
GRANT 4	MAS	CHANNEL 4	YES
GRANT 5	MAS	CHANNEL 5	YES
GRANT 6	MAS	CHANNEL 6	YES
GRANT 7	MAS	CHANNEL 7	YES
GRANT 8	MAS	MBI 0	YES
GRANT 9	MAS	MBI 1	YES

TABLE IV. MSM Memory Bus Signals (Cont)

SIGNAL(S)	SOURCE	DESTINATION	UNIDIRECTIONAL?
GRANT 10	MAS	MBI 2	YES
GRANT 11	MAS	MBI 3	YES
TYPE	ALL CHANNELS AND MBI's	MAS	YES
$\overline{\text{READ}}$	ALL CHANNELS AND MBI's	MAS	YES
$\overline{\text{WRITE}}$	ALL CHANNELS AND MBI's	MAS	YES
$\overline{\text{GRANT SYNC}}$	ALL CHANNELS AND MBI's	MAS	YES
ADDRESS OF 0-16	ALL CHANNELS AND MBI's	MAS	YES
DATA 0-35 AND PARITY BITS	ALL CHANNELS AND MBI's	MAS & SSM	NO
WORD MODE	ALL CHANNELS	MAS	YES
WORD SELECT	ALL CHANNELS	MAS	YES
BYTE MODE	ALL CHANNELS	MAS	YES
BYTE SELECT	ALL CHANNELS	MAS	YES
$\overline{\text{DATA LATCH}}$	MAS	ALL CHANNELS & MBI's	YES
$\overline{\text{TIME OUT ERROR}}$	MAS	ALL MBI's	YES

TABLE V. ICS I/O Bus Signals

SIGNAL(S)	SOURCE(S)	DESTINATION(S)	FUNCTIONS
$\overline{\text{SEIZE}}$	IOBI	CHANNELS 0-7	SEIZE CHAN IF CHAN SELECTS HI.
$\overline{\text{RELEASE}}$	IOBI	CHANNELS 0-7	RELEASE CHAN IF CHAN SELECTS HI.
$\overline{\text{CPU 0 RLS}}$	IOBI	CHANNELS 0-7	RELEASE ALL CHANS SEIZED BY CPU 0
$\overline{\text{CPU 1 RLS}}$	IOBI	CHANNELS 0-7	RELEASE ALL CHANS SEIZED BY CPU 1
$\overline{\text{CPU 2 RLS}}$	IOBI	CHANNELS 0-7	RELEASE ALL CHANS SEIZED BY CPU 2
$\overline{\text{CPU 3 RLS}}$	IOBI	CHANNELS 0-7	RELEASE ALL CHANS SEIZED BY CPU 3
CHANNEL SEL'S (3)	IOBI	CHANNELS 0-7	SELECTS CHAN FOR DATA TRANSFER
REGISTER SEL'S (9)	IOBI	CHANNELS 0-7	SELECTS REGISTER FOR DATA TRANSFER
$\overline{\text{WRITE}}$	IOBI	CHANNELS 0-7	WRITES DATA TO CHANNEL REGISTER
$\overline{\text{READ}}$	IOBI	CHANNELS 0-7	READS DATA FROM CHANNEL REGISTER
ENABLE DATA	IOBI	CHANNELS 0-7	ENABLES DATA FOR WRITE
$\overline{\text{PI LEVEL RESET}}$	IOBI	CHANNELS 0-7	RESETS PI LEVEL REGISTERS IN CHANNEL

TABLE V. ICS I/O Bus Signals (Cont)

SIGNAL(S)	SOURCE(S)	DESTINATION(S)	FUNCTION
ICS DATA BUS (16)	IOBI	CHANNELS 0-7	BIDRECTIONAL 16 BIT DATA BUS
DEC-10 KEEP ALIVE	IOBI	CHANNELS 0-7	TELLS SEIZED CHAN's CPU STILL OPERATING
SEL PI LEVEL (3)	IOBI	CHANNELS 0-7	PI LEVEL DEC-10 HAS RECOGNIZED
CHAN 0 SEL	IOBI	CHANNEL 0	ENABLES CHAN 0 TO BE SEIZED OR RELEASED IF HI
CHAN 1 SEL	IOBI	CHANNEL 1	ENABLES CHAN 1 TO BE SEIZED OR RELEASED IF HI
CHAN 2 SEL	IOBI	CHANNEL 2	ENABLES CHAN 2 TO BE SEIZED OR RELEASED IF HI
CHAN 3 SEL	IOBI	CHANNEL 3	ENABLES CHAN 3 TO BE SEIZED OR RELEASED IF HI
CHAN 4 SEL	IOBI	CHANNEL 4	ENABLES CHAN 4 TO BE SEIZED OR RELEASED IF HI
CHAN 5 SEL	IOBI	CHANNEL 5	ENABLES CHAN 5 TO BE SEIZED OR RELEASED IF HI
CHAN 6 SEL	IOBI	CHANNEL 6	ENABLES CHAN 6 TO BE SEIZED OR RELEASED IF HI
CHAN 7 SEL	IOBI	CHANNEL 7	ENABLES CHAN 7 TO BE SEIZED OR RELEASED IF HI

TABLE V. ICS I/O Bus Signals (Cont)

SIGNAL(S)	SOURCE(S)	DESTINATION(S)	FUNCTIONS
I/O REGISTER O READ	CHANNELS 0-7	IOBI	RESETS DEC-10 KEEP ALIVE BIT
PI 1-7 (7)	CHANNELS 0-7	IOBI	INTERRUPTS THE SEIZING DEC-10
CHANNEL 0 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 0	IOBI	TELLS SEIZED STATUS OF CHANNEL 0
CHANNEL 1 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 1	IOBI	TELLS SEIZED STATUS OF CHANNEL 1
CHANNEL 2 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 2	IOBI	TELLS SEIZED STATUS OF CHANNEL 2
CHANNEL 3 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 3	IOBI	TELLS SEIZED STATUS OF CHANNEL 3
CHANNEL 4 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 4	IOBI	TELLS SEIZED STATUS OF CHANNEL 4
CHANNEL 5 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 5	IOBI	TELLS SEIZED STATUS OF CHANNEL 5

TABLE V. ICS I/O Bus Signals (Cont)

SIGNAL(S)	SOURCE(S)	DESTINATION(S)	FUNCTIONS
CHANNEL 6 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 6	IOBI	TELLS SEIZED STATUS OF CHANNEL 6
CHANNEL 7 SEIZED BY THIS OR ANOTHER CPU (2)	CHANNEL 7	IOBI	TELLS SEIZED STATUS OF CHANNEL 7
CHANNEL 0 INTERRUPTING ON SELECT LEVEL	CHANNEL 0	IOBI	TELLS WHETHER CHANNEL 0 IS INTERRUPTING
CHANNEL 1 INTERRUPTING ON SELECT LEVEL	CHANNEL 1	IOBI	TELLS WHETHER CHANNEL 1 IS INTERRUPTING
CHANNEL 2 INTERRUPTING ON SELECT LEVEL	CHANNEL 2	IOBI	TELLS WHETHER CHANNEL 2 IS INTERRUPTING
CHANNEL 3 INTERRUPTING ON SELECT LEVEL	CHANNEL 3	IOBI	TELLS WHETHER CHANNEL 3 IS INTERRUPTING
CHANNEL 4 INTERRUPTING ON SELECT LEVEL	CHANNEL 4	IOBI	TELLS WHETHER CHANNEL 4 IS INTERRUPTING
CHANNEL 5 INTERRUPTING ON SELECT LEVEL	CHANNEL 5	IOBI	TELLS WHETHER CHANNEL 5 IS INTERRUPTING

TABLE V. ICS I/O Bus Signals (Cont)

SIGNAL(S)	SOURCE(S)	DESTINATION(S)	FUNCTIONS
CHANNEL 6 INTERRUPTING ON SELECT LEVEL	CHANNEL 6	IOBI	TELLS WHETHER CHANNEL 6 IS INTERRUPTING
CHANNEL 7 INTERRUPTING ON SELECT LEVEL	CHANNEL 7	IOBI	TELLS WHETHER CHANNEL 7 IS INTERRUPTING

TABLE VI. PDP-11 to SSM Addressing Characteristics and Bit Utilization

INTERLEAVED?	WORD MODE	MAX # OF SSM PAGES ADDRESSABLE	# OF SSM WORDS/ PAGE/MSI	PDP-11 SELECT BITS				
				PAGE	WORD	MSI	HALF WORD	BYTE
NO	1-1	248*	512	10-17	1-9	-	-	0
NO	2-1	124+	512	11-17	2-10	--	1	0
YES	1-1	248	128†	10-17	3-9	1-2	-	0
YES	2-1	124	128	11-17	4-10	2-3	1	0

* PDP-11 CAN ACCESS 124K WORDS MAX; 124K WORDS/512 WORDS/PAGE = 248 PAGES

+ IN 2-1 MODE EACH PAGE HOLDS 1024 PDP-11 WORDS OR 1K; 124K WORDS/1K WORDS/PAGE = 124 PAGES

† IN INTERLEAVED MODE EACH PAGE IS CONTAINED IN 4MSI's; 512 WORDS/PAGE/4MSI's = 128 WORDS/PAGE/MSI

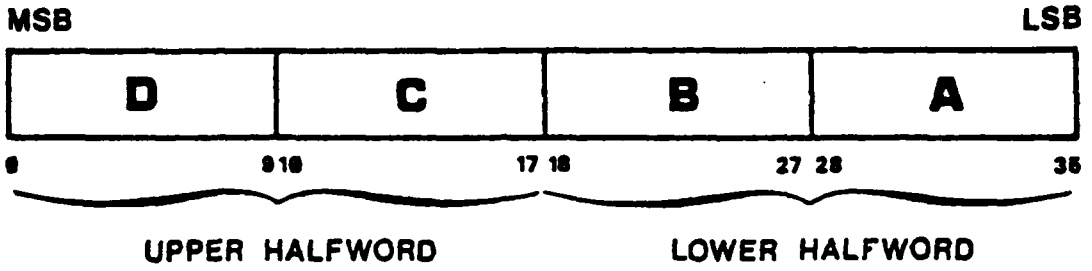

Figure 18 SSM Word Format

TABLE VII. Front Panel/Diagnostic Correlation

FRONT PANEL		DIAGNOSTIC	
SECTION	LIGHTS	NAME	SECTION
MSM CHANNEL MONITOR	INTERRUPT	INTERACTIVE INTERRUPT TEST	4.1.2.4.3 4.1.2.4.4
		GENERAL REGISTER TEST	4.1.2.5.1
	PDP-11 BASE ADDRESS	INTERACTIVE INTERRUPT TEST	4.1.2.4.3 4.1.2.4.4
		GENERAL REGISTER	4.1.2.5.1
	SEIZING I/O BUS	SEIZING TEST	4.1.2.3.1
	PAGE LIMIT	PAGE LIMIT REGISTER TEST	4.1.2.3.3
		MEMORY TRANSFER TEST	4.1.2.4.4
		GENERAL REGISTER TEST	4.1.2.5.1
IOBI MONITOR	CHANNEL SEIZED	SEIZING TEST	4.1.2.3.1
		GENERAL REGISTER TEST	4.1.2.5.1
	ACTIVE PI LEVELS	MEMORY TRANSFER TEST	4.1.2.4.4
	PI LEVEL LAST SERVICED	MEMORY TRANSFER TEST	4.1.2.4.4
	PDP-11's INTERRUPTING ON LEVEL LAST SERVICED	MEMORY TRANSFER TEST	4.1.2.4.4

TABLE VII. Front Panel/Diagnostic Correlation (Cont)

FRONT PANEL		DIAGNOSTIC	
SECTION	LIGHTS	NAME	SECTION
MAS MONITOR	PORTS REQUESTING SERVICE	MEMORY TRANSFER TEST	4.1.2.4.4
	PORT LAST SERVICED	MEMORY TRANSFER TEST	4.1.2.4.4
	LAST OPERATION	ZERO TEST	4.1.2.2.1
		MEMORY TRANSFER TEST	4.1.2.4.4

TABLE VIII. Verification Cross Reference Index

SUBSYSTEM		DIAGNOSTIC	
NAME	SECTION	NAME	SECTION
MEMORY SUB-SYSTEM	3.2.1.1	ZERO TEST	4.1.2.2.1
		ONES TEST	4.1.2.2.2
		ADDRESS TEST	4.1.2.2.3
		DUAL ADDRESSING TEST	4.1.2.2.4
		MEMORY TRANSFER TEST	4.1.2.4.4
MSM MEMORY BUS	3.2.1.2	ZERO TEST	4.1.2.2.1
		ONES TEST	4.1.2.2.2
		DUAL ADDRESSING TEST	4.1.2.2.4
INTERPROCESSOR COMMUNICATIONS SUBSYSTEM	3.2.1.3	SEIZING TEST	4.1.2.3.1
		MEMORY MAPPING RAM TEST	4.1.2.3.2
		PAGE LIMIT REGISTER TEST	4.1.2.3.3
		FUNCTION REGISTER TEST	4.1.2.3.4
		INTERACTIVE FUNCTION REGISTER TEST	4.1.2.4.1
		INTERACTIVE INTERRUPT TESTS	4.1.2.4.2 4.1.2.4.3
		MEMORY TRANSFER TEST	4.1.2.4.4
		NON-EXISTANT MEMORY TEST	4.1.2.5.2

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10.0 APPENDIX I MSM Registers Accessed by DEC-10

Below is a summary of the MSM registers accessable by the DEC-10 and their physical location within MSM. The detail bit definitions for these registers are on the following pages.

ICC

MAC

IOBI

MSM COMMAND DEVICE 1 (LOCATED IN IOBI)

A CONO INSTRUCTION FROM THE DEC-10 TO THE FIRST OF TWO MSM DEVICE CODES COMMANDS ACTION IN AN ICC OR IN THE IOBI.

BIT	FUNCTION
18	SEIZE CONTROL OF CHANNELS 0-7 SELECTED BY BITS 20-27
19	RELEASE CONTROL OF CHANNELS 0-7 SELECTED BY BITS 20-27
20-27	CHANNEL SELECT: CHANNEL 0=BIT 27 CHANNEL 7=BIT 20
28	RESET THE IOBI
29	RELEASE ALL CHANNELS FROM CONTROL OF CPU-3
30	RELEASE ALL CHANNELS FROM CONTROL OF CPU-2
31	RELEASE ALL CHANNELS FROM CONTROL OF CPU-1
32	RELEASE ALL CHANNELS FROM CONTROL OF CPU-0
35	KEEP ALIVE BIT SIGNIFIES THAT CPU IS RUNNING

MSM STATUS DEVICE 1 (LOCATED IN IOBI)

A CONI INSTRUCTION TO THE FIRST OF TWO MSM DEVICE CODES READS IN STATUS INFORMATION ABOUT THE PDP-11 CHANNELS.

BIT	FUNCTION
20-27	CHANNELS WHICH ARE SEIZED BY THIS CPU PDP-11 0=BIT 27
28-35	CHANNELS WHICH ARE SEIZED BY ANOTHER CPU PDP-11 0=BIT 35
18	MEMORY IS ON LINE = 0 OFF LINE = 1
1-5	MEMORY SIZE IN NUMBER OF 16K BLOCKS
6-13	STARTING ADDRESS OF MEMORY (16K DEC-10 BOUNDARY)
14-15	IOBI NUMBER ASSIGNMENT (0-3)

MSM STATUS DEVICE 2 (LOCATED IN IOBI)

A CONI INSTRUCTION TO THE SECOND OF TWO MSM DEVICE CODES IS USED FOR READING IN INTERRUPT STATUS.

BIT	FUNCTION
21-28	PDP-11's WHICH ARE INTERRUPTING ON THE SELECTED PI CHANNEL PDP-11 #7 = BIT 21
29	INTERRUPT PRESENT ON PI LEVEL 7
30	INTERRUPT PRESENT ON PI LEVEL 6
31	INTERRUPT PRESENT ON PI LEVEL 5
32	INTERRUPT PRESENT ON PI LEVEL 4
33	INTERRUPT PRESENT ON PI LEVEL 3
34	INTERRUPT PRESENT ON PI LEVEL 2
35	INTERRUPT PRESENT ON PI LEVEL 1

MSM DATA OUT DEVICE 1 (LOCATED IN IOBI)

THE DATA OUT DEVICE IS LOADED WITH A DATAO INSTRUCTION AND USED TO LOAD DATA TO CHANNEL REGISTERS. THE DATAO SPECIFIES THE CHANNEL, THE REGISTER, AND THE DATA. THE CHANNEL REGISTERS CAN ONLY BE LOADED IF THE DEC-10 HAS FIRST SEIZED CONTROL OF THE ICC FOR THE CHANNEL BEING SELECTED BY BITS 5-7 (EXCEPT FOR CERTAIN INTERRUPT CONTROL AND STATUS REGISTERS). THE FIRST MSM DEVICE CODE MUST BE SELECTED FOR REGISTER ADDRESS.

BITS	FUNCTIONS
0	IF "1" ENABLES SELECTION OF THE CHANNEL USING BITS 5-7. ONCE THE CHANNEL HAS BEEN SELECTED, IT WILL REMAIN SELECTED UNTIL ANOTHER DATAO COMMAND SELECTS A DIFFERENT ONE BY SENDING A NEW SELECTION CODE WITH BIT 0 SET.
1	IF "1", 16 BITS OF DATA FROM BITS 20-35 WILL BE LOADED INTO THE SELECTED REGISTER IF 0, NO DATA IS LOADED (USED TO SELECT A REGISTER FOR THE NEXT DATAI)
5-7	CHANNEL SELECT CODE IF BIT 0 IS SET (BIT 7 = LSB)
9-17	REGISTER SELECT CODE (BIT 17 = LSB)
20-35	DATA TO BE WRITTEN INTO SELECTED REGISTER IF BIT 1 IS SET (BIT 35 = LSB).

MSM DATA IN DEVICE 1 (LOCATED IN IOBI)

THE CHANNEL REGISTERS ARE READ BY A DATAI INSTRUCTION.
THE REGISTER MUST FIRST BE SELECTED WITH A DATAO INSTRUCTION.

BITS	FUNCTION
5-7	CHANNEL SELECT CODE
9-17	REGISTER SELECT CODE
20-35	16 BITS OF DATA

DEC-10 ACCESSIBLE REGISTERS

OCTAL REGISTER NUMBER(S)	DATAO/DATAI BITS	REGISTER DEFINITION
0-367		MEMORY MAPPING RAM,
	23	INVALID PAGE = 1
	24	WRITE-PROTECTED PAGE = 1
	25	SIGN EXTEND = 1
	26-35	10-BIT MSM MEMORY PAGE
400		BASE ADDRESS (READ ONLY)
	31-35	5-BIT 4K BOUNDARY, SWITCH SELECTABLE (PDP-11 START ADDRESS)
401		PAGE LIMIT/ADDRESS MODE
	28-35	8-BIT NUMBER OF THE MEMORY MAPPING RAM WORD THAT IS THE FIRST WORD AFTER THE LAST VALID WORD IN THE RAM (0_8 IF NONE VALID, 370_8 IF ALL ARE VALID), = 248_{10} PAGES
	20	1=1-1 MODE, 0=2-1 MODE
402		PDP-11 COMMAND AND STATUS REGISTER 1 (A)
	28-31	IOBI NUMBER WHICH HAS CONTROL (READ) 0=NONE, BIT 31 = CPU 0 BIT 28 - CPU 3
	32	ICC ON LINE = 1
	33	PDP-11 POWER ON (READ) = 1
	34	PDP-11 KEEP ALIVE (READ) = 1 (WILL RESET IF CPU HAVING SEIZED CONTROL READS THE REGISTER)
	35	RESET THE ICC (WRITE)

DEC-10 ACCESSIBLE REGISTERS (CONT)

OCTAL REGISTER NUMBER(S)	DATAO/DATAI BITS	REGISTER DEFINITION
403		PDP-11 COMMAND AND STATUS REGISTER 2
	26	CLEAR INTERRUPT REQUEST FROM PDP-11 (WRITE)
	27	DEC-10 INTERRUPT ENABLE (READ & WRITE)
	28	PDP-11 INTERRUPT ENABLE (READ)
	29	ENABLE SETTING OF PI LEVELS FOR INTERRUPTING THE DEC-10 (WRITE)
	30-32	PI LEVEL B (READ AND WRITE) 1-7 PI LEVEL 0 NONE
	33-35	PI LEVEL A (READ AND WRITE) 1-7 PI LEVEL 0 NONE
404		PDP-11 INTERRUPT ADDRESS
	29-35	7-BIT INTERRUPT ADDRESS FOR INTERRUPTING THE PDP-11 (READ & WRITE)
405		PDP-11 INTERRUPT LEVEL (WRITE)
	33-35	3-BIT BR LEVEL FOR INTERRUPTING THE PDP-11 (WRITING TO THIS REGISTER STARTS INTERRUPT)

DEC-10 ACCESSIBLE REGISTERS (CONT)

OCTAL REGISTER NUMBER(S)	DATAO/DATAI BITS	REGISTER DEFINITION
406	20-35	FUNCTION REGISTER 1 16-BIT GENERAL PURPOSE REGISTER WHICH BOTH DEC-10 AND PDP-11 CAN READ OR WRITE
407	20-35	FUNCTION REGISTER 2 16-BIT GENERAL PURPOSE REGISTER WHICH BOTH DEC-10 AND PDP-11 CAN READ OR WRITE

NOTE: ANY DEC-10 CAN READ COMMAND AND STATUS REGISTER #1 AT ANYTIME. HOWEVER, IN ORDER TO RESET THE ICC, THE DEC-10 MUST FIRST HAVE SEIZED CONTROL OF THE ICC. (BIT 35)

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20.0 APPENDIX II MSM Registers Accessed by PDP-11

Below is a summary of the MSM registers accessable by PDP-11's. These registers are addressed in the 4K I/O page of the PDP-11 addressing space. The I/O base address is selected with switches in the PDP-11 interface (DUC). Detailed bit definitions of these are shown on the following pages.

(NOTE: PDP-11 conventions are Bit 0 = LSB, Bit 15 = MSB) These registers are physically located in the ICC.

COMMAND REGISTER (I/O BASE ADDRESS)

LOADED WITH A MOV INSTRUCTION TO THE REGISTER ADDRESS.

BITS	FUNCTION
15	ENABLE ERROR INTERRUPT OF PDP-11 (ERROR VECTOR SELECTED WITH DIP SWITCHES IN DUC)
14	CLEAR MEMORY PARITY ERROR FLAG
13	CLEAR WRITE PROTECTION VIOLATION FLAG
3	PDP-11 KEEP ALIVE
2	ENABLE INTERRUPT OF PDP-11
1	INTERRUPT THE DEC-10 ON PI LEVEL B
0	INTERRUPT THE DEC-10 CPU ON PI LEVEL A

STATUS REGISTER (I/O BASE ADDRESS)

READ WITH A MOV INSTRUCTION FROM THE REGISTER ADDRESS.

BIT	FUNCTION
0	DEC-10 PRIORITY A INTERRUPT ENABLE (A NON-ZERO PI CHANNEL HAS BEEN ASSIGNED, INTERRUPTS ARE ENABLED, AND AN INTERRUPT FROM THIS PDP-11 IS NOT IN PROGRESS)
1	DEC-10 PRIORITY B INTERRUPT ENABLE (SAME AS BIT 0)
2	PDP-11 INTERRUPT ENABLE
9	KEEP-ALIVE-BIT-DEC-10 CPU IS RUNNING (BIT 9 RESETS WHEN THIS REGISTER IS READ)
10	MSM POWER IS ON
13	WRITE PROTECTION VIOLATION ERROR FLAG
14	MEMORY PARITY ERROR FLAG
15	PDP-11 ERROR INTERRUPT ENABLE

INTERRUPT VECTOR (I/O BASE ADDRESS + 2)

READ WITH A MOV INSTRUCTION FROM THE REGISTER ADDRESS.

(DEC-10 ACCESSIBLE REGISTER # 404)

BITS	FUNCTION
6-0	7-BIT VECTOR TRAP ADDRESS SET BY DEC-10 CPU FOR INTERRUPTS TO THE PDP-11, BIT 6 = MSB BIT 0 = LSB

BASE ADDRESS (I/O BASE ADDRESS + 4)

READ WITH A MOV INSTRUCTION FROM THE REGISTER ADDRESS.

BITS	FUNCTION
4-0	5-BIT 4K PDP-11 ADDRESS BOUNDARY WHERE PDP-11 BEGINS ADDRESSING THE MSM MEMORY BIT 4 = MSB, BIT 0 = LSB (SELECTED BY DIP SWITCHES IN ICC)

- - PAGE LIMIT/ADDRESS MODE (I/O BASE ADDRESS + 6)

READ WITH A MOV INSTRUCTION FROM THE REGISTER ADDRESS.

(DEC-10 ACCESSIBLE REGISTER #401)

BIT	FUNCTION
7-0 15	8-BIT NUMBER OF THE MEMORY MAPPING RAM WORD THAT IS ONE GREATER THAN THE LAST VALID WORD IN THE RAM. BIT 7 = MSB, BIT 0 = LSB 0=2-1 MODE; 1=1-1 MODE

FUNCTION REGISTER 1 (I/O BASE ADDRESS + 10_8)

READ WITH A MOV INSTRUCTION, WRITE WITH A MOV INSTRUCTION.

(DEC-10 ACCESSIBLE REGISTER #406)

BITS	FUNCTION
15-0	16 BITS OF READ OR WRITE DATA

FUNCTION REGISTER 2 (I/O BASE ADDRESS + 12_8)

READ WITH A MOV INSTRUCTION; WRITE WITH A MOV INSTRUCTION

(DEC-10 ACCESSIBLE REGISTER #407)

BITS	FUNCTION
15-0	16 BITS OF READ OR WRITE DATA

30.0 APPENDIX III Flowcharts for MSM Diagnostics

AD-A126 634 CRITICAL ITEM PRODUCT FUNCTION SPECIFICATION FOR THE MULTIPROCESSOR SHARE..(U) AIR FORCE WRIGHT AERONAUTICAL LABS WRIGHT-PATTERSON AFB OH J A LUKE ET AL. JAN 83

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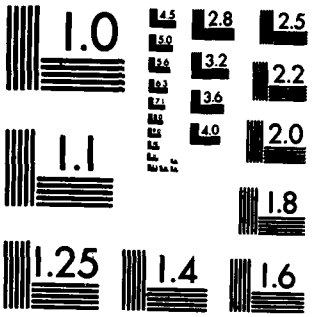
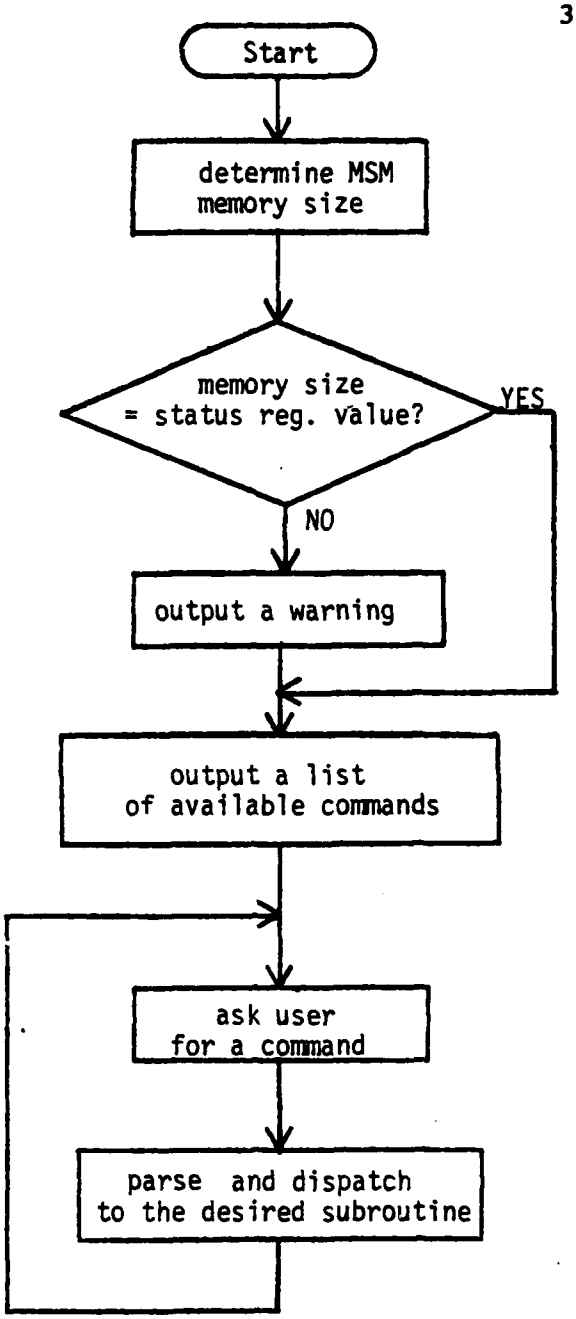
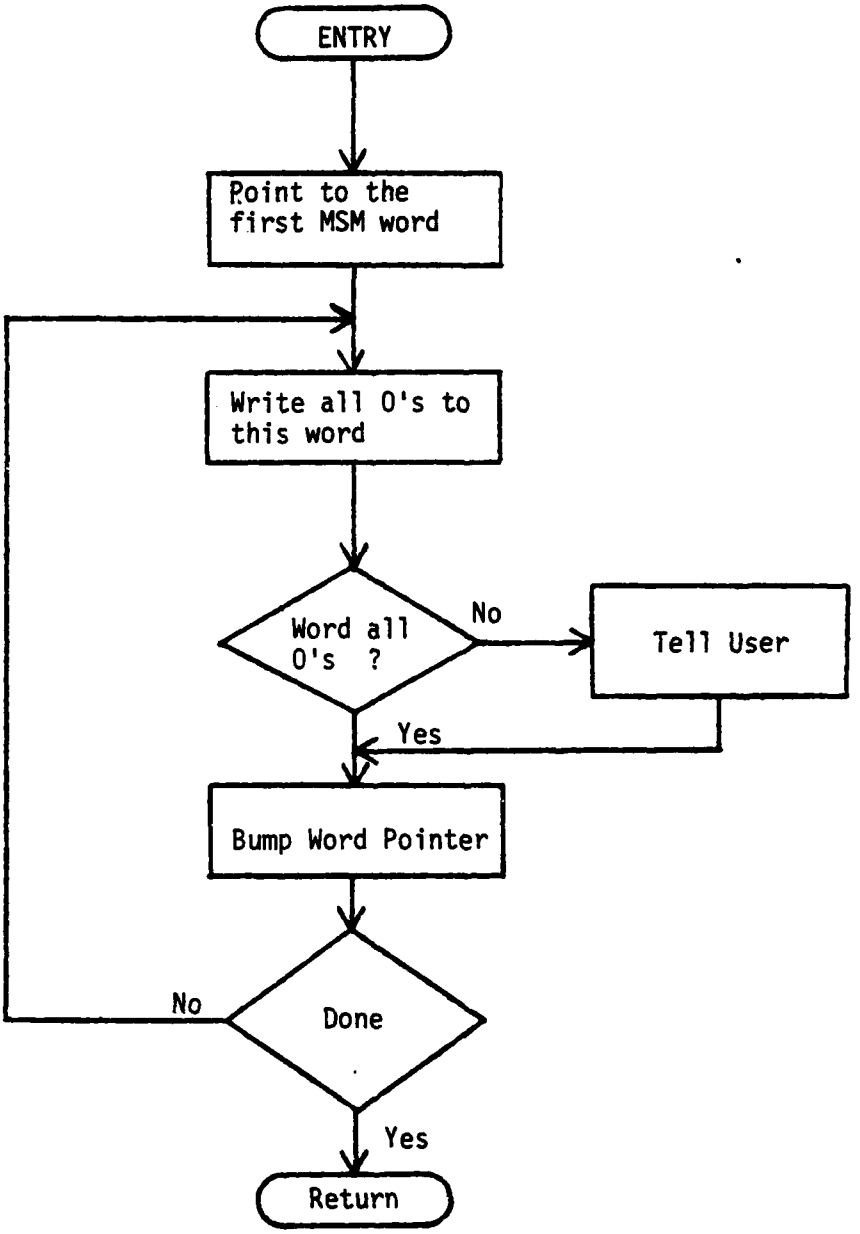
DTIC

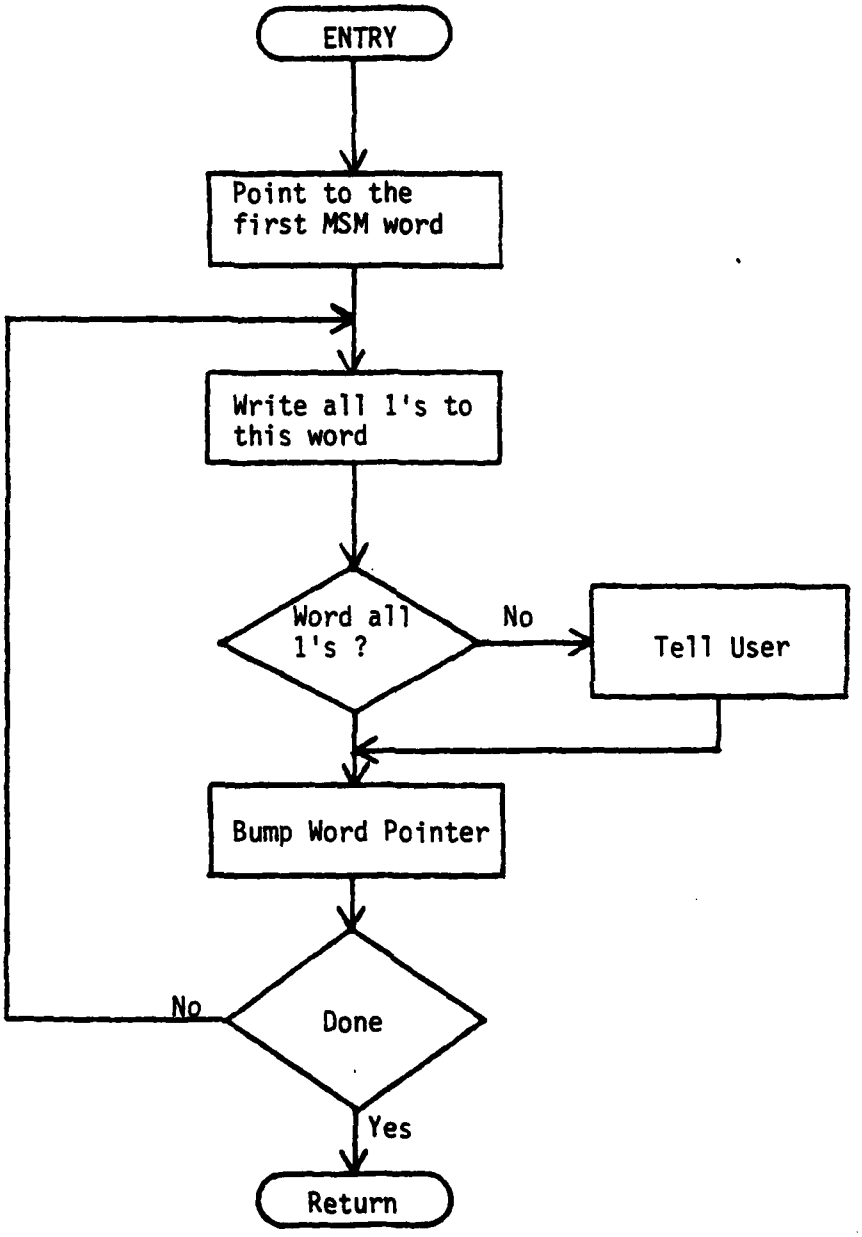




Initialization

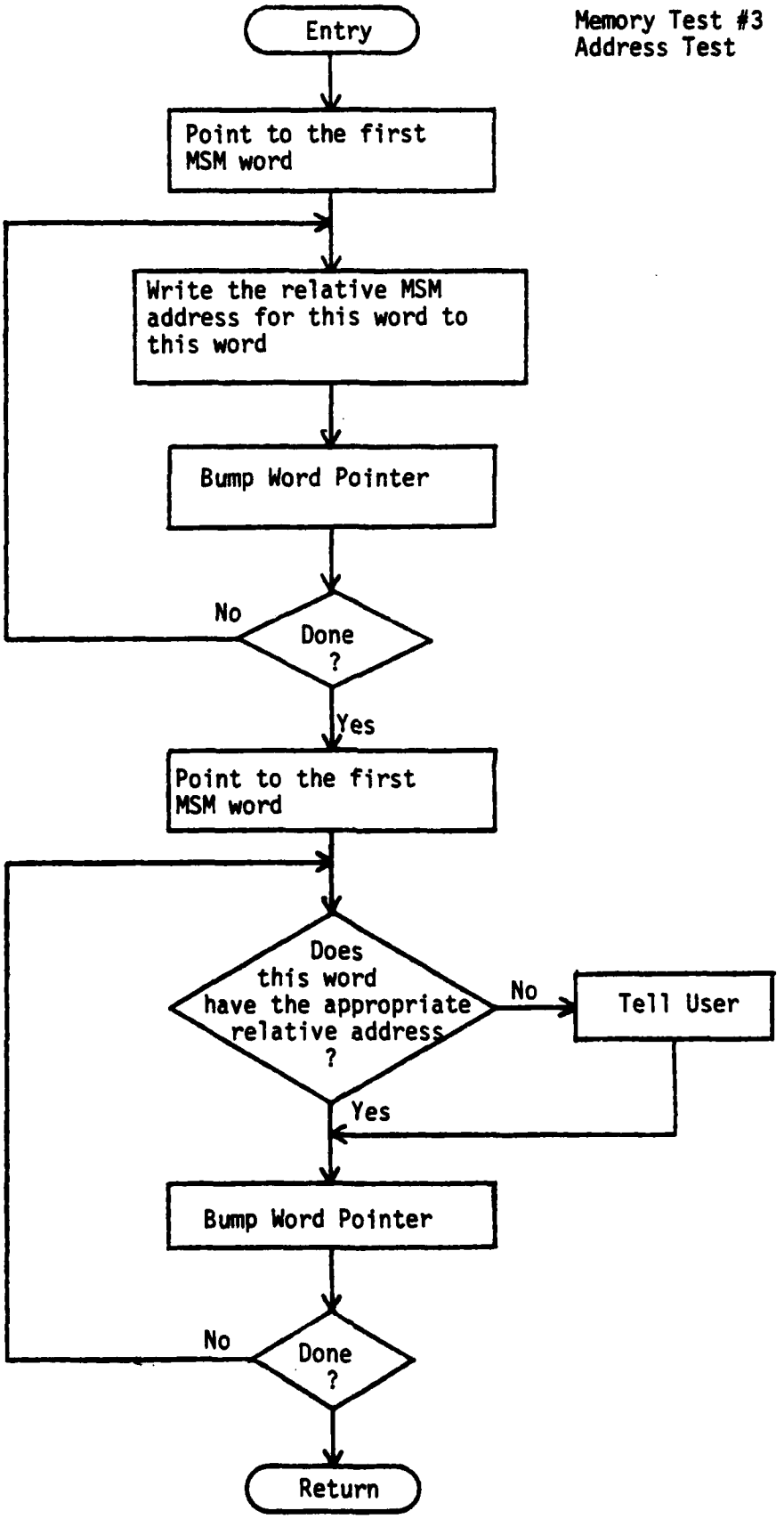


Memory Test #1
Zero Test

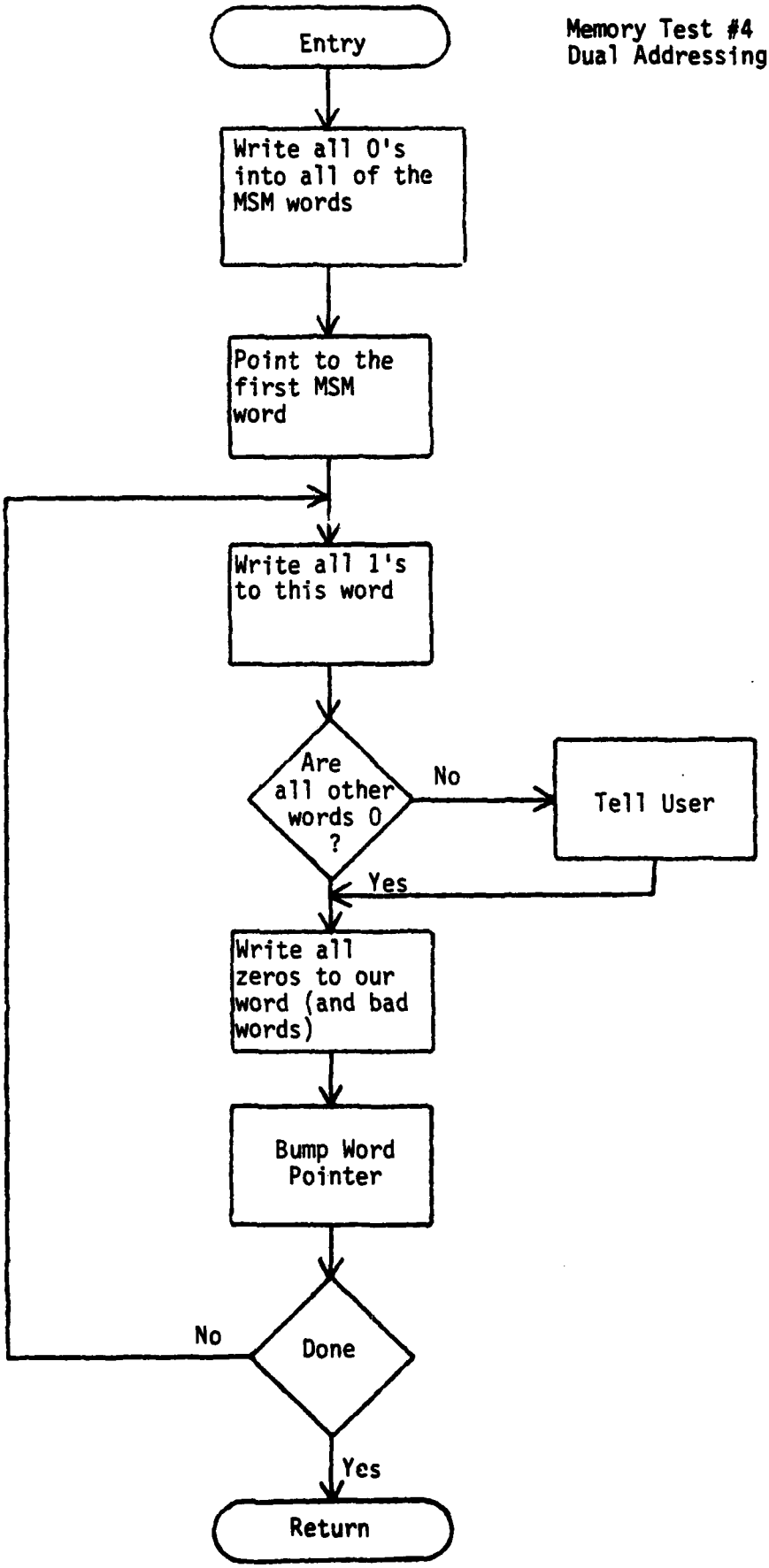


Memory Test #2
Ones Test

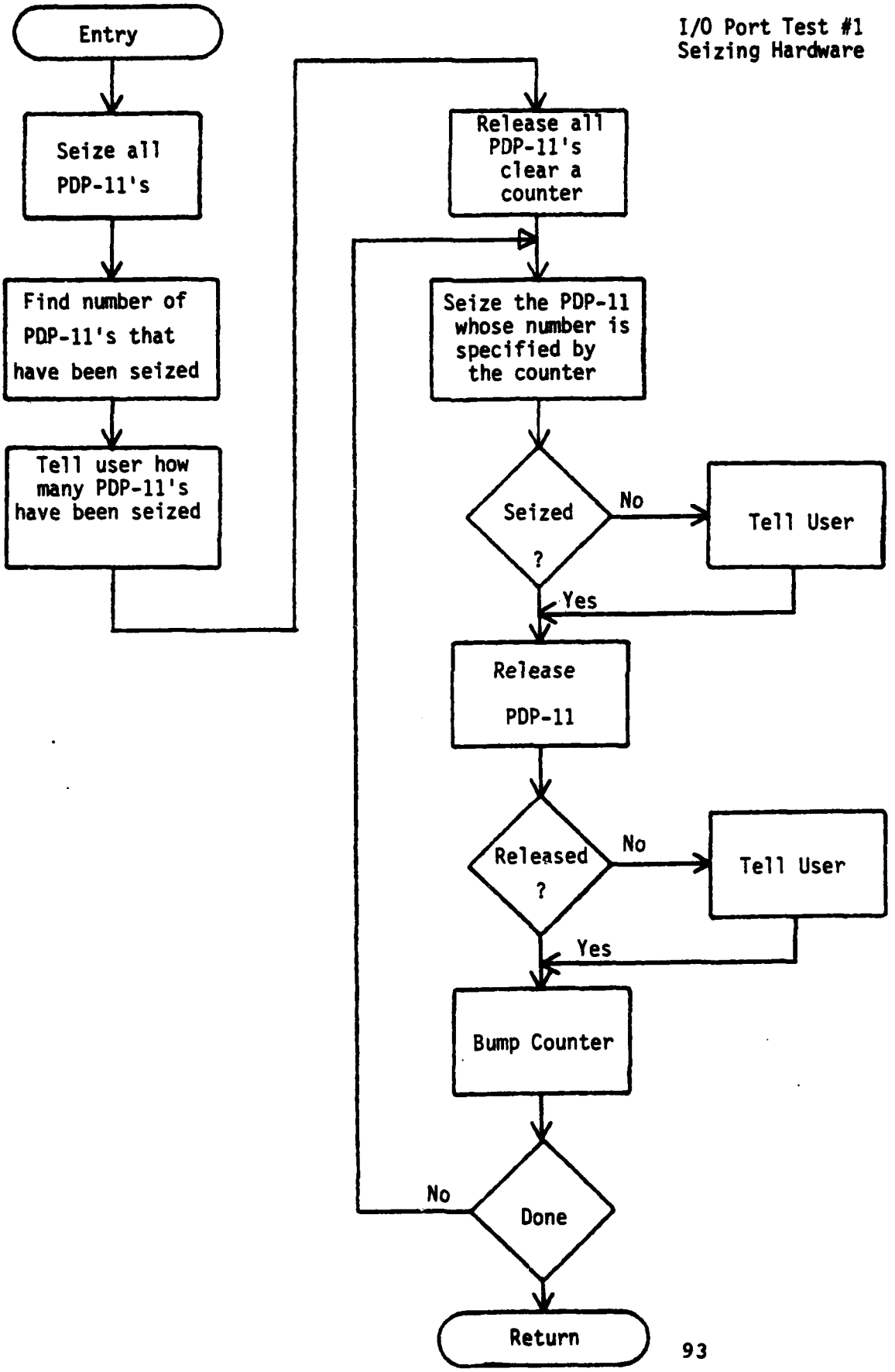
Memory Test #3
Address Test

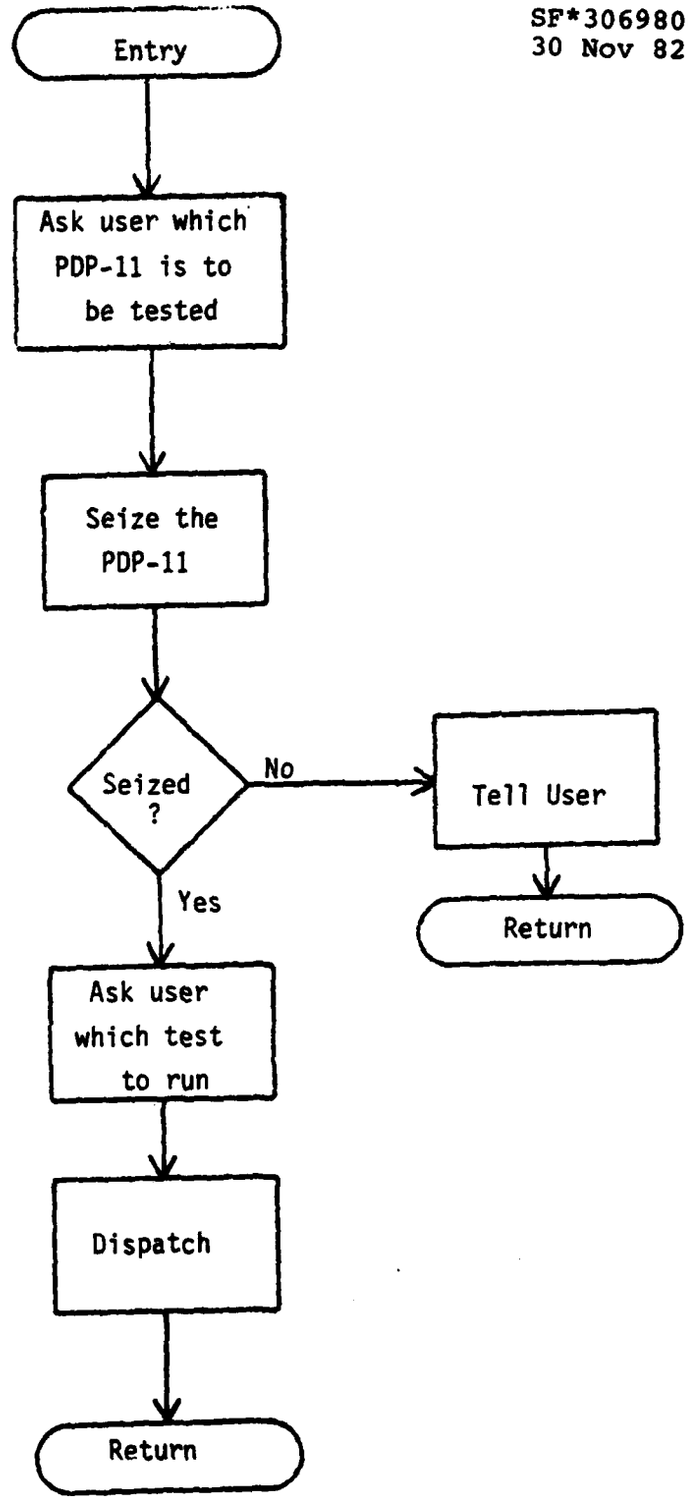


Memory Test #4
Dual Addressing Test

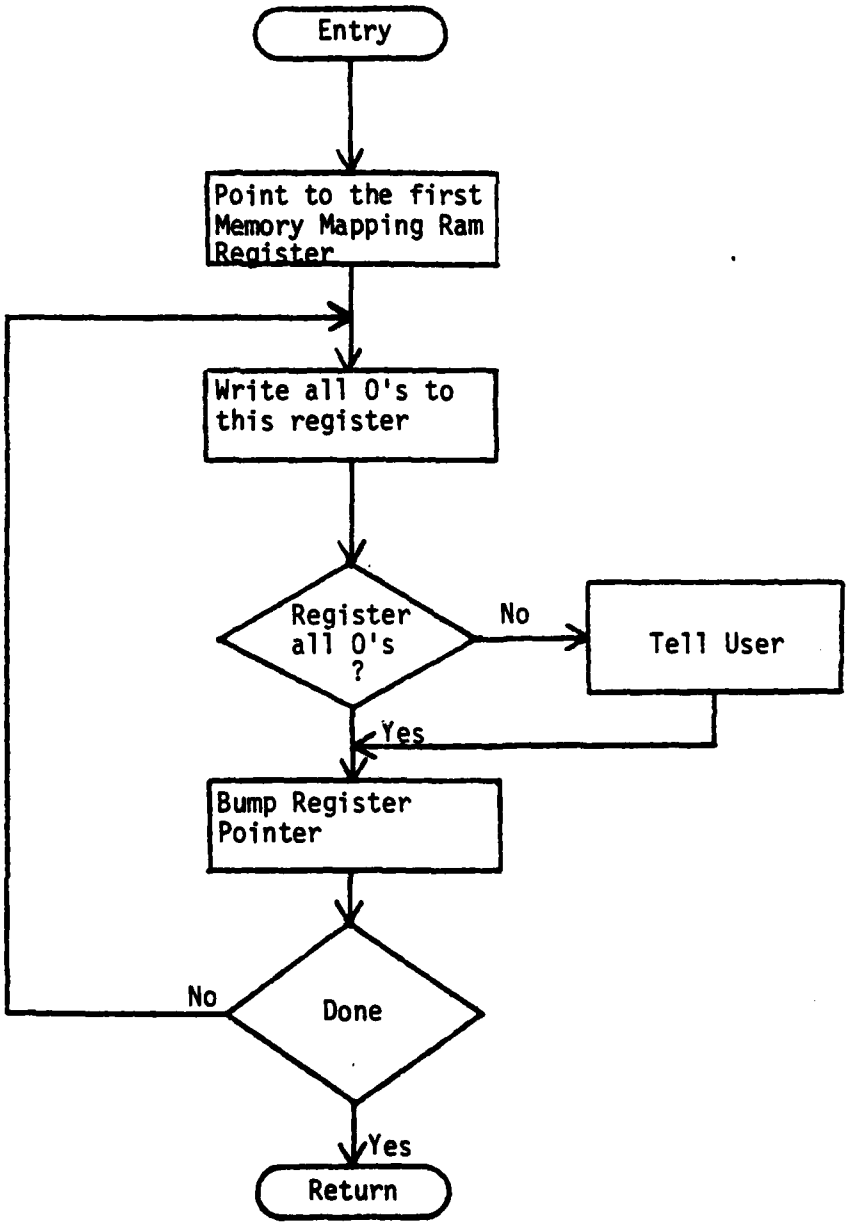


I/O Port Test #1
Seizing Hardware

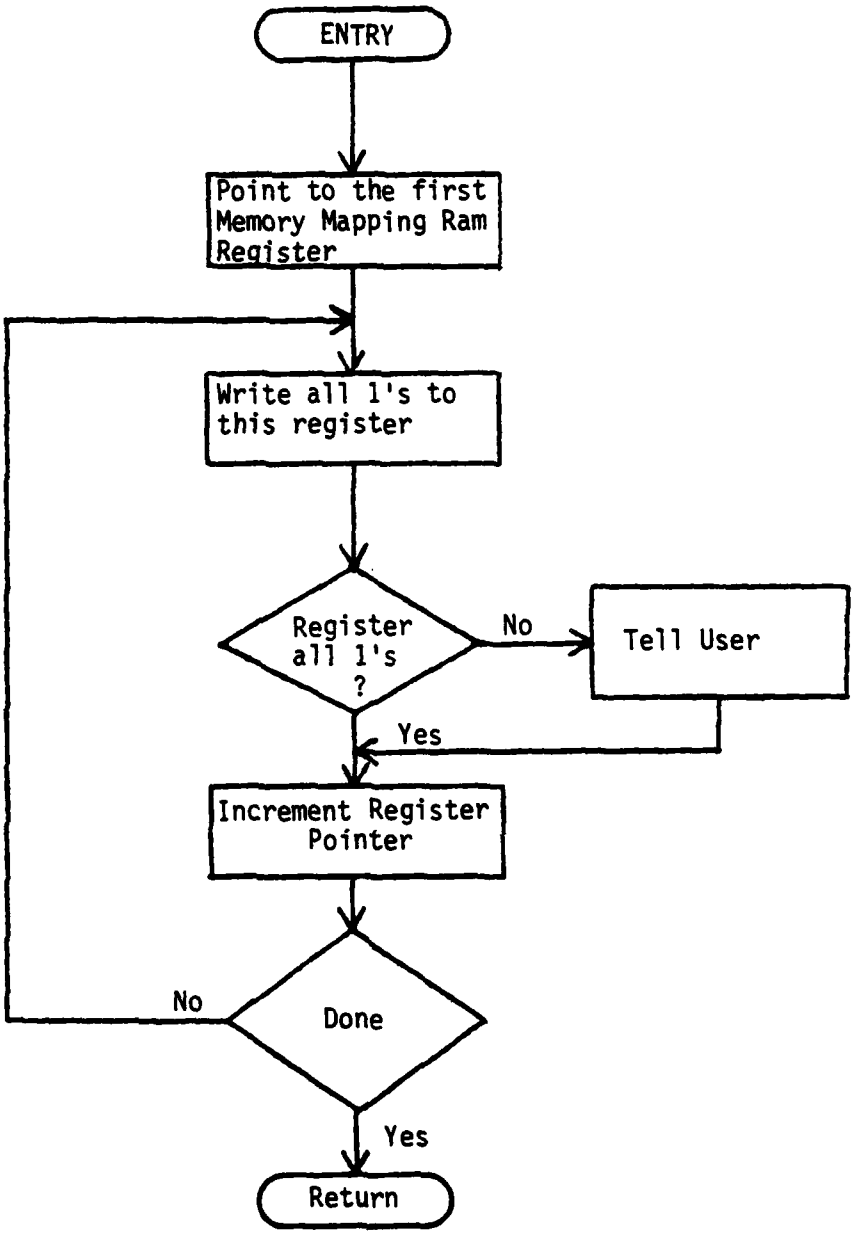




I/O Port Test #2 Register Tests

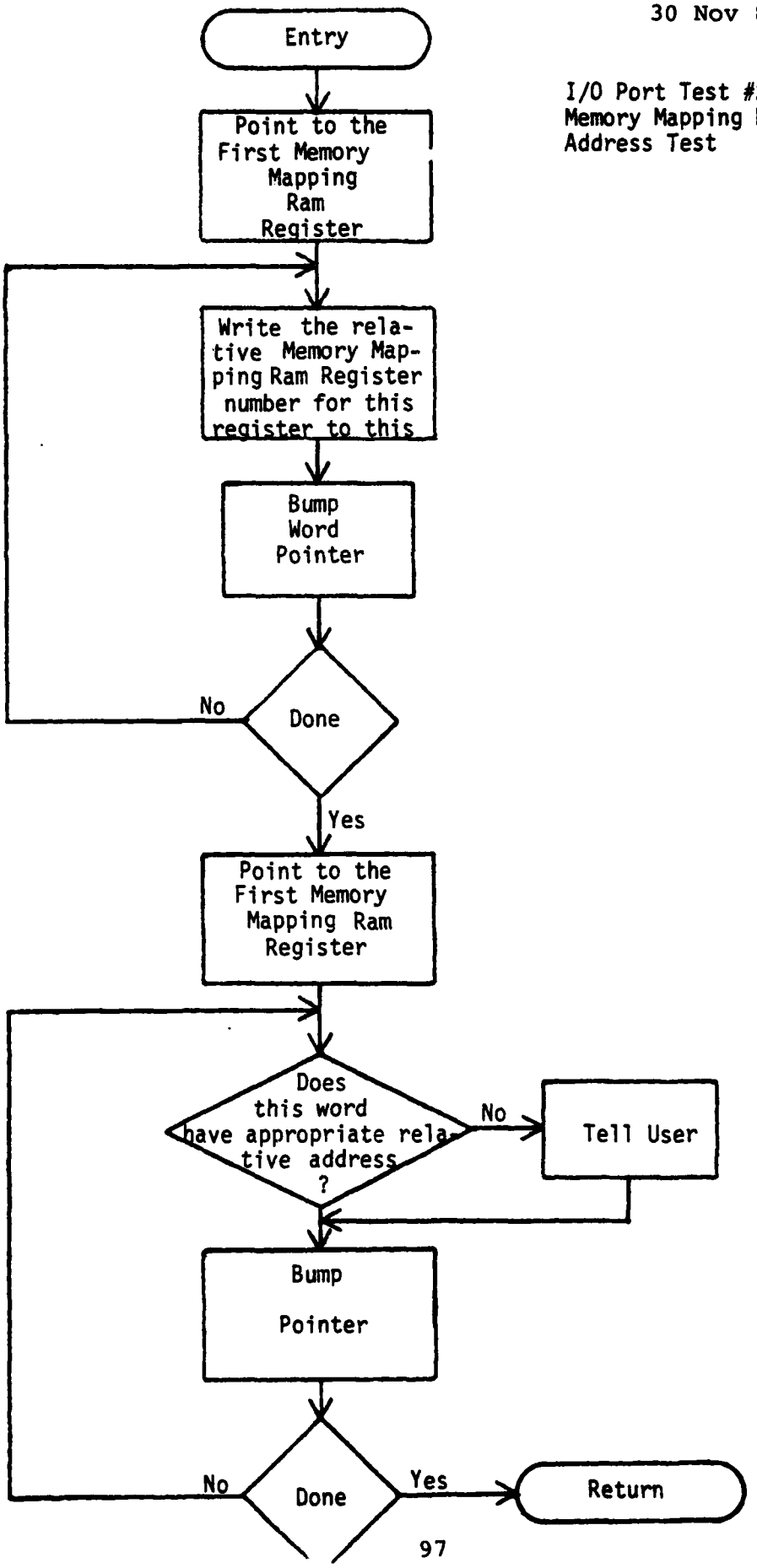


I/O Port Test #2a
Memory Mapping Ram Test
Zero Test

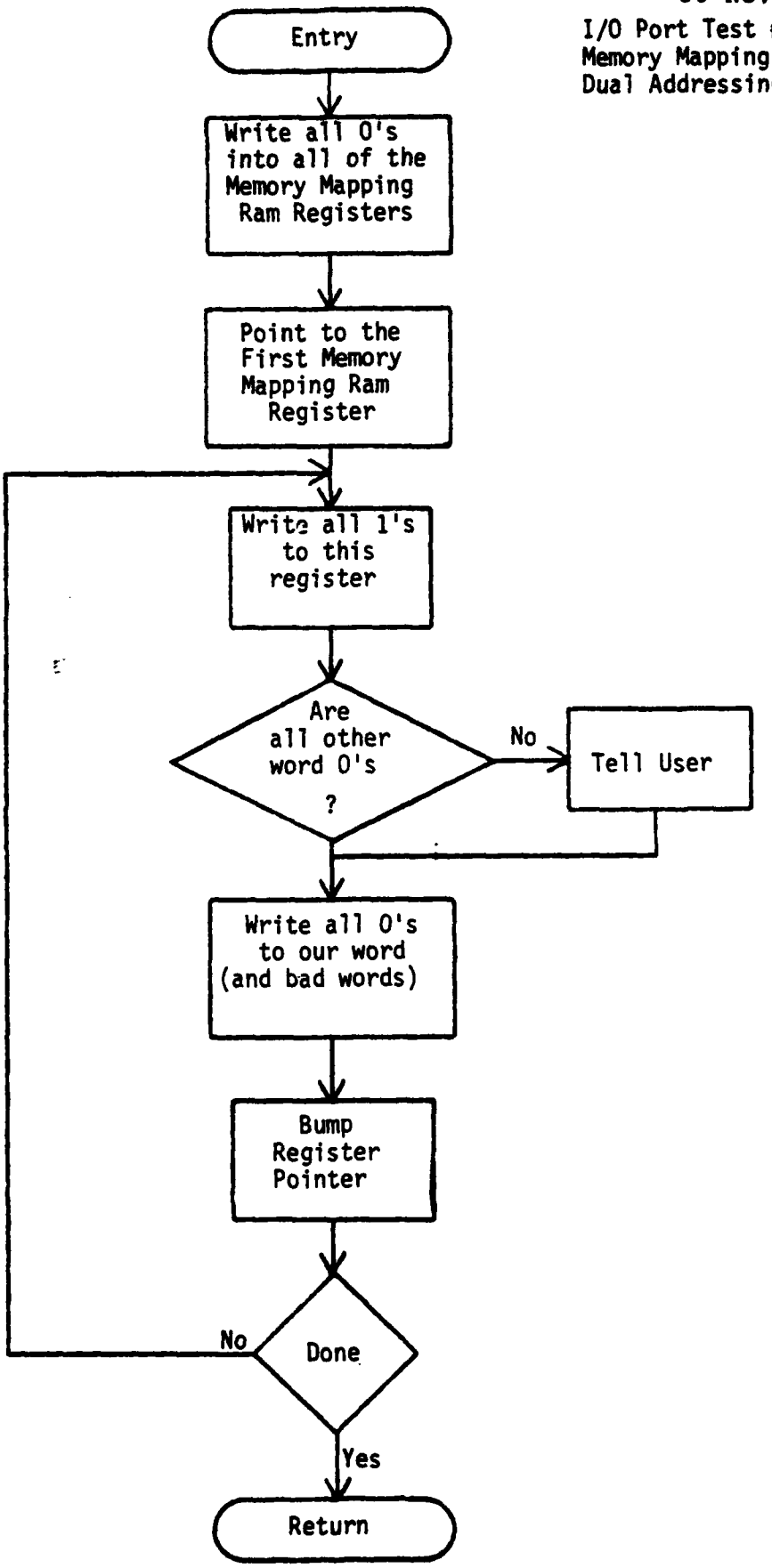


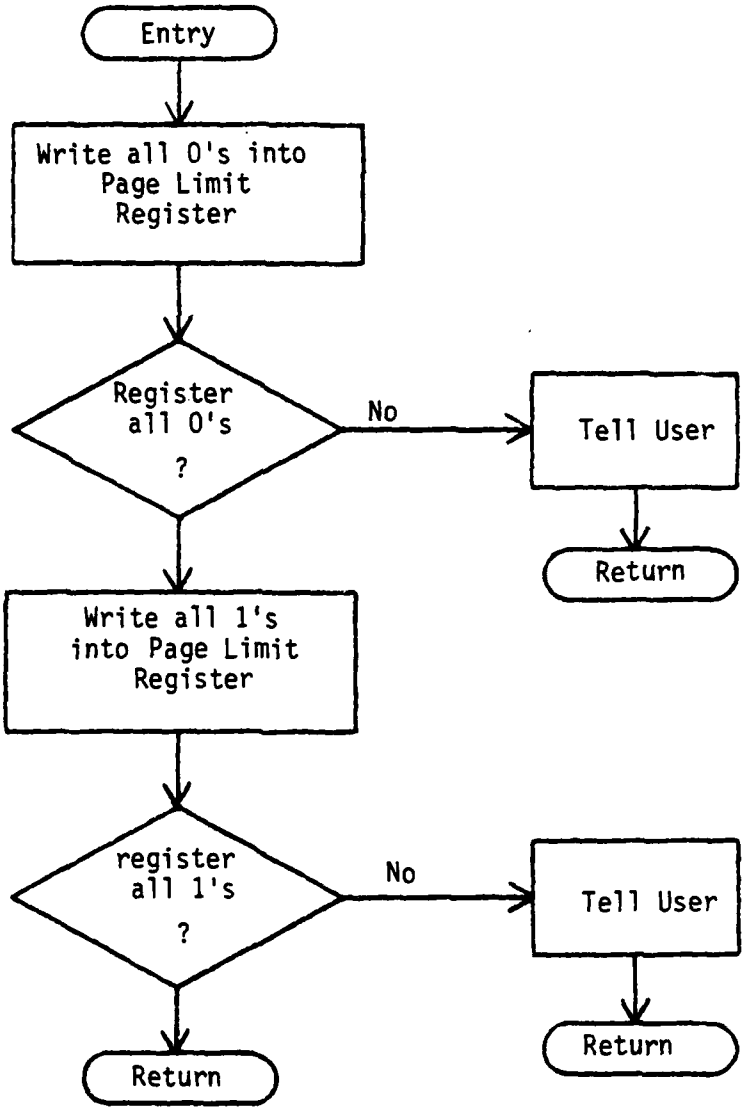
I/O Port Test #2b
Memory Mapping Ram Test
Ones Test

I/O Port Test #2c
Memory Mapping Ram Test
Address Test



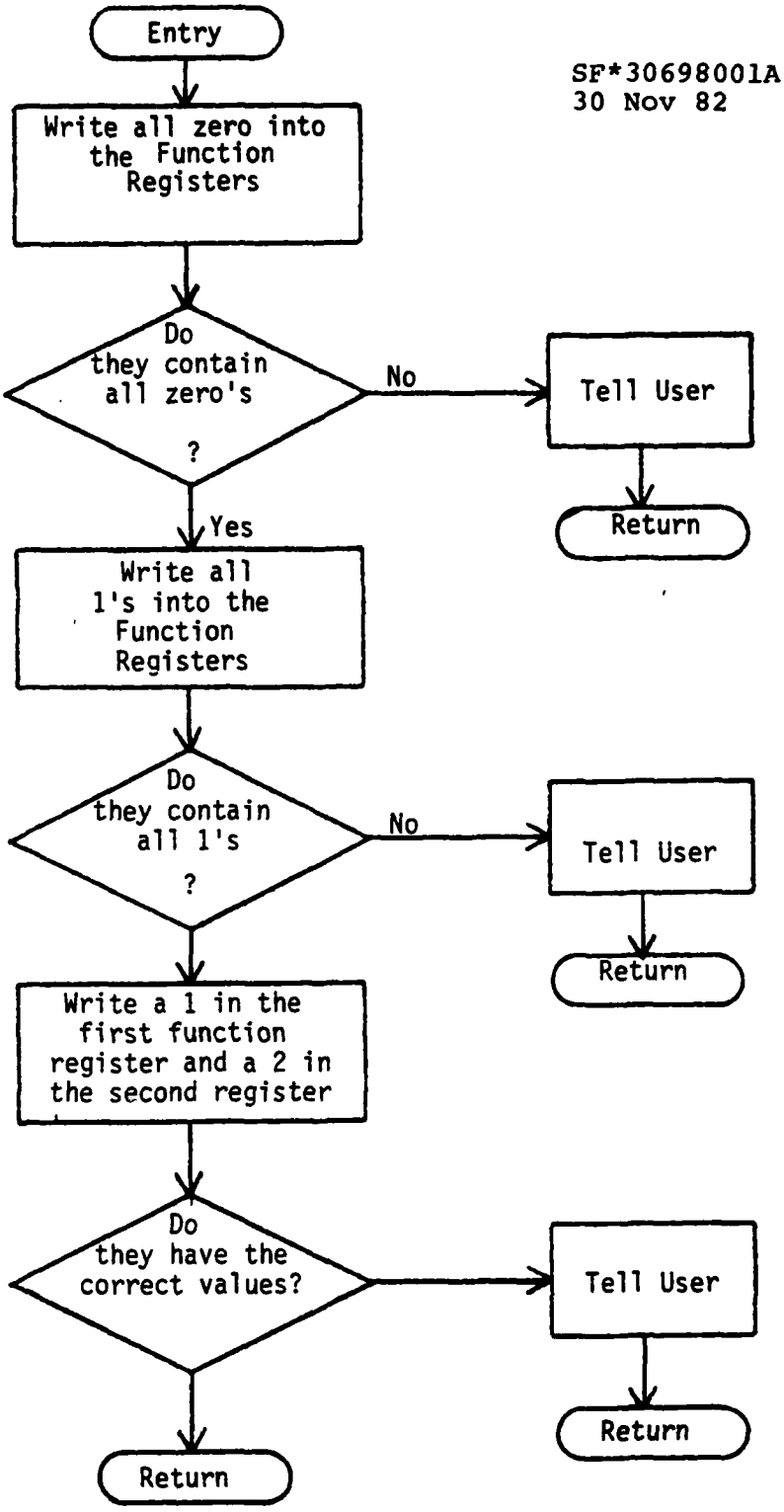
I/O Port Test #2d
Memory Mapping Ram Test
Dual Addressing Test



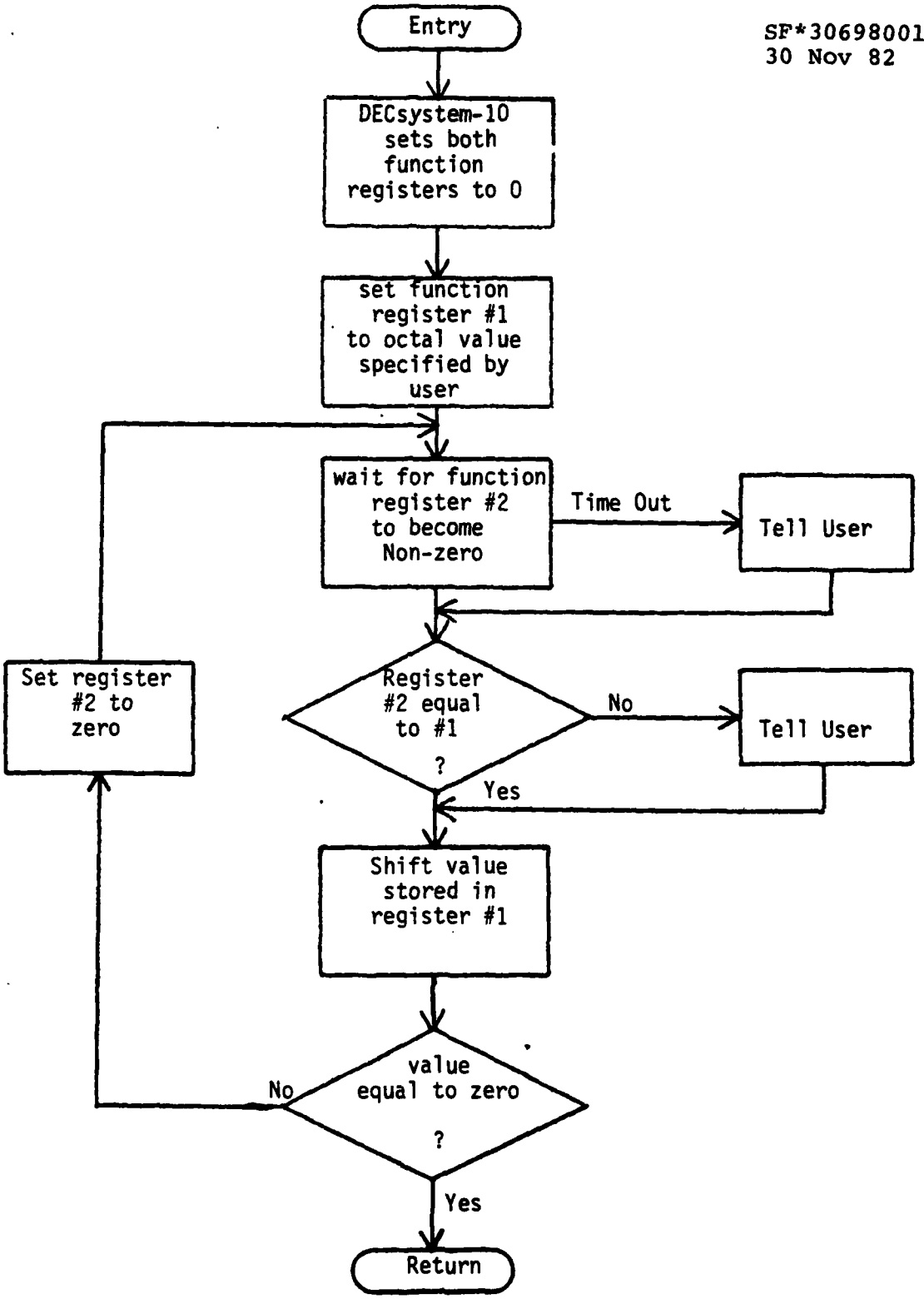


I/O Port Test #2e
Page Limit Register

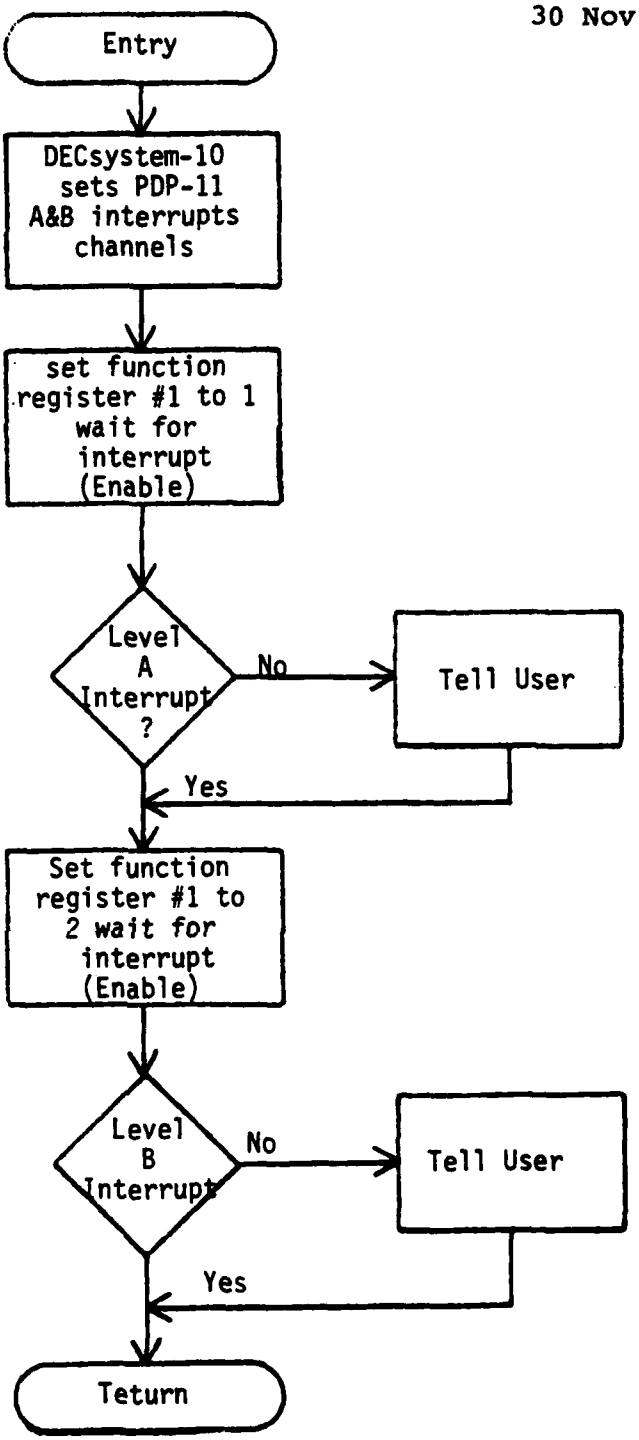
SF*30698001A
30 Nov 82



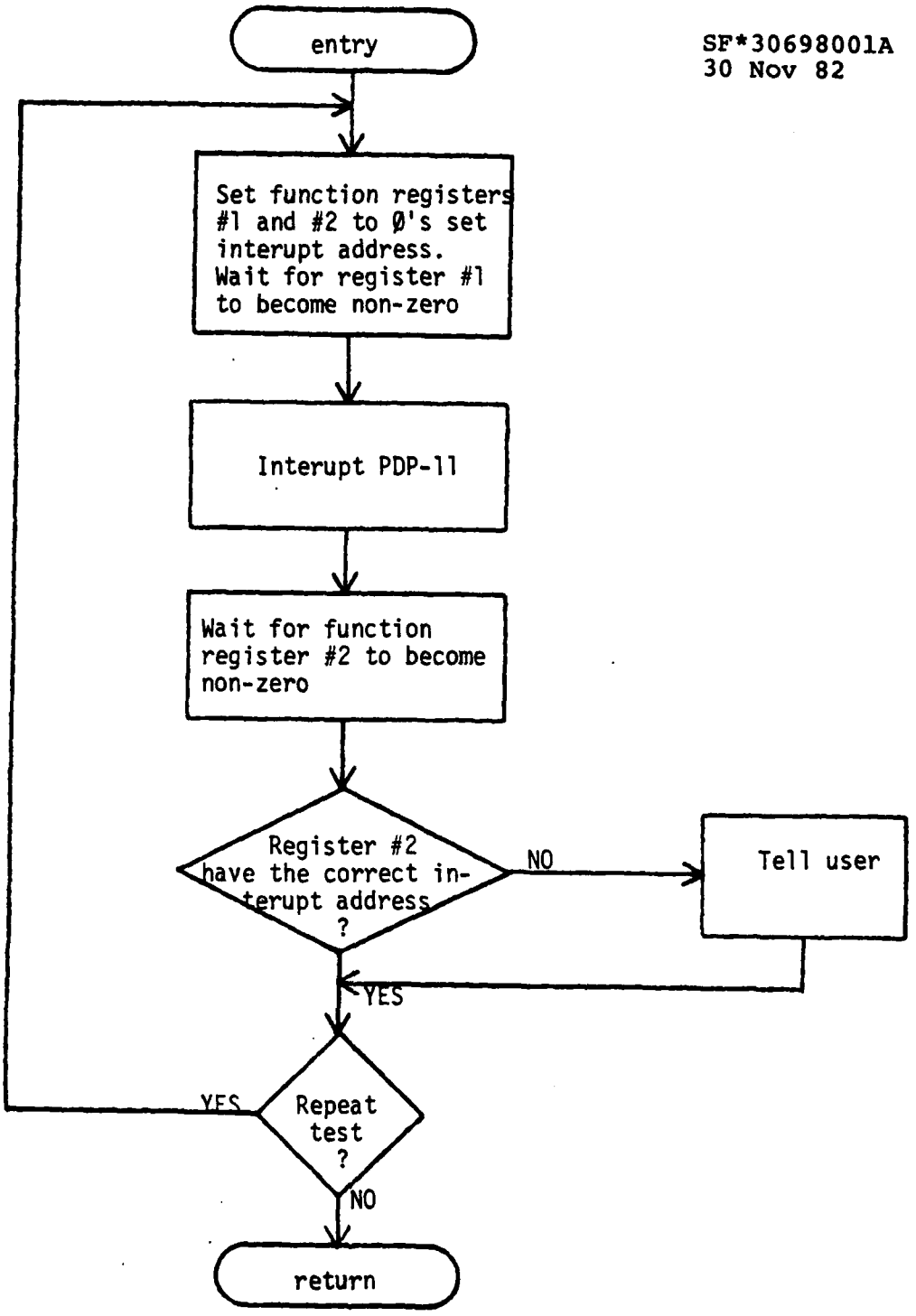
I/O Port Test #2f
Function Registers



Interactive Test #1
Function Register

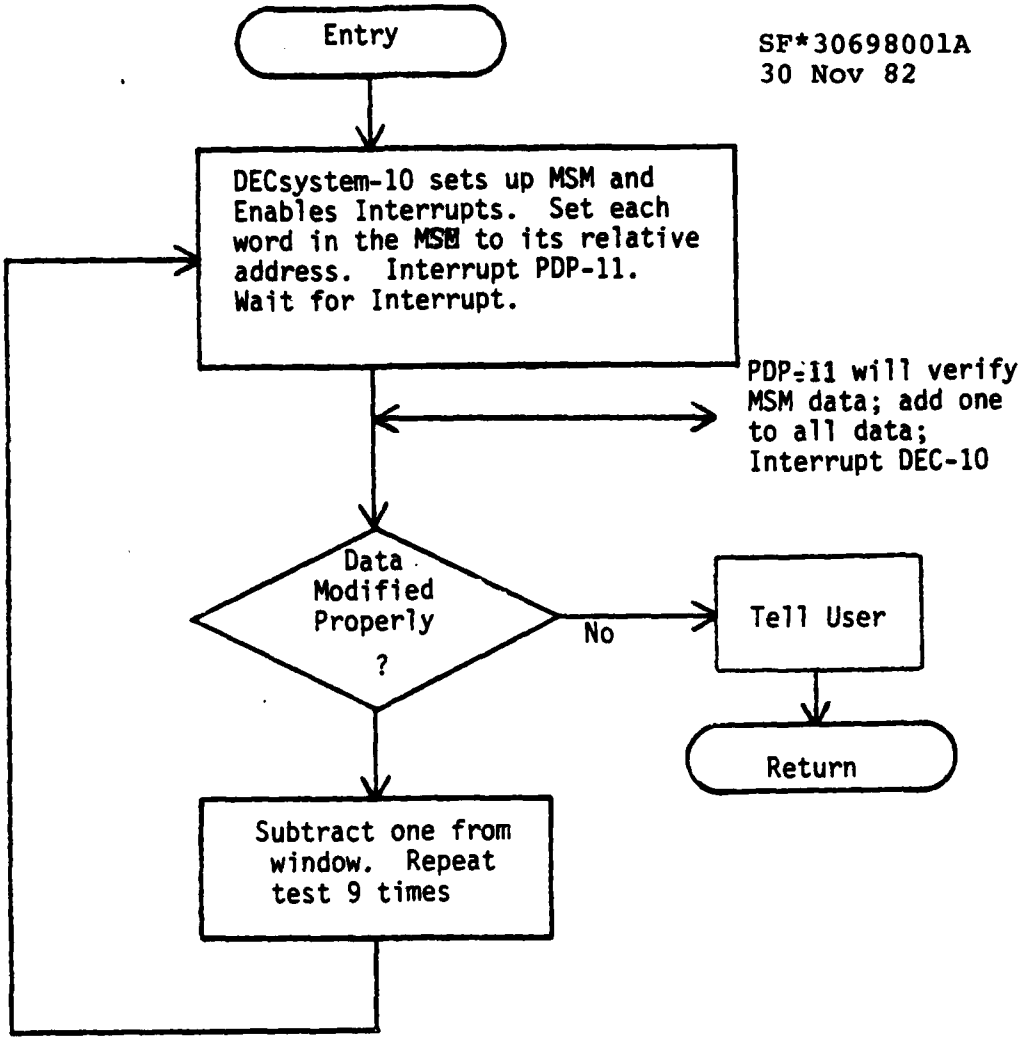


Interactive Test #2
Interrupts



Interactive Test #2a
Interrupts

SF*30698001A
30 Nov 82



Interactive Test #3
Memory Transfer

40.0 APPENDIX IV List of Acronyms and Abbreviations

The following are lists of acronyms and abbreviations used in this Specification. Note that references to PDP-11 in this document mean the use of a UNIBUS-compatible device. DEC-10 is synonomous with DECsystem-10

40.1 Multiprocessor Shared Memory

DUC - Differential UNIBUS Converter
ICC - Interprocessor Communications Controller
ICS - Interprocessor Communications Subsystem
IOBI - I/O Bus Interface
MAC - Memory Access Controller
MAS - Memory Access Sequencer
MBI - Memory Bus Interface
MS - Memory Subsystem
MSFPL - Memory Status and Front Panel Logic
MSI - Memory, Sequencer, and Interface
MSM - Multiprocessor Shared Memory
SCS - Status and Control Subsystem
SSM - Solid State Memory

40.2 DEC-10 Processor I/O Instruction

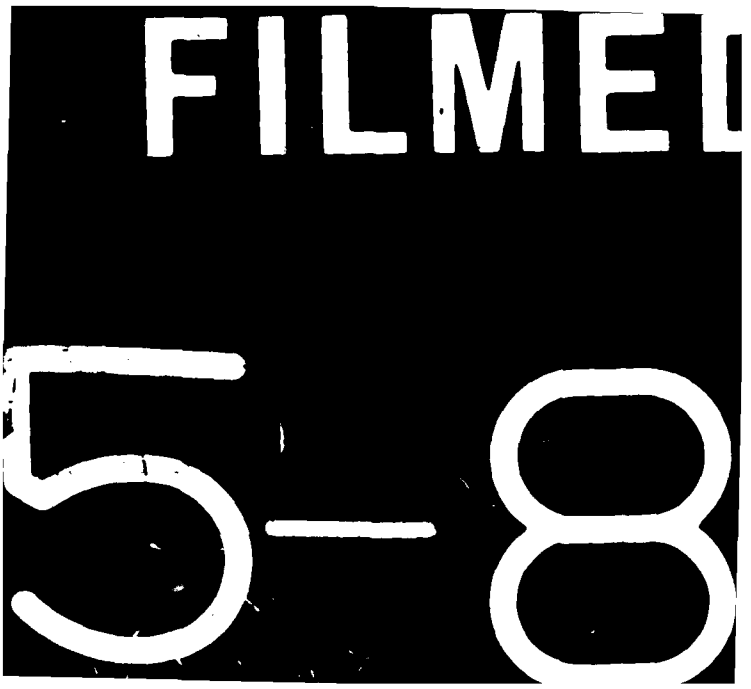
CONI - Condition In
CONO - Condition Out
DATAI - Data In
DATAO - Data Out

40.3 PDP-11 Processor Instruction

MOV - Move

40.4 General

CPU - Central Processing Unit
HMOS - High-Performance Metal-Oxide-Semiconductor
I/O - Input/Output
RAM - Random Access Memory
IC - Integrated Circuit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5-8